Proceedings of XVIII Workshop on

Semiconductors and Micro & Nano Technology - 2024

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ISBN: 978-65-01-03636-6

PREFACE

This volume contains the papers presented at SEMINATEC 2024: XVIII Workshop on Semiconductors and Micro & Nano Technology on April 18—19, 2024. The SEMINATEC 2024 edition took place at Polytechnic School of the University of São Paulo.

In 2024 the SEMINATEC was organized by Electron Devices Society (EDS) of IEEE South Brazil chapter, Laboratory of Integrable Systems at Polytechnic School (LSI/PSI) of the University of São Paulo (USP), and São Paulo State University (UNESP).

There were 43 submissions selected for poster presentation at SEMINATEC 2024 as well as the presentations of 6 invited talks, all of them distinguished lecturers of the IEEE:

1) Cor Claeys, ClaRoo, Belgium
   Title: Advanced Semiconductor Technology and Device Architectures for the Next Decade.
2) Antonio Cerdeira Altuzarra, Center of Research and Advanced Studies, Mexico.
   Title: Modeling FinFETs, Nanowires and Nanosheets
3) Magali Estrada, Center of Research and Advanced Studies, Mexico
   Title: 2D semiconductor FET transistors: Characteristics, fabrication and modelling
4) Deji Akinwande, University of Texas – Austin, USA
   Title: Novel Applications of 2D Materials from AI/Memory Devices to 6G Switches to Wearable Sensors
5) Adelmo Ortiz-Conde, Universidad Simón Bolívar, Venezuela
   Title: Recent Applications of the Lambert's W function to device modeling
6) Alberto Valdes Garcia, IBM, USA
   Title: 3D millimeter-wave imaging and sensing with Si-based phased arrays, edge computing, and AI

We also had a Pannel about "Federal Government Semiconductor Policy", a round table about "Teaching Microelectronics in Brazil" and the Industrial Section with the presentations of Cadence, OKK/Tektronix and Keysight.

We would like to thank for the financial support got from the EDS/IEEE South Brazil chapter, EDS Student Chapter of UNICAMP, EDS Student Chapter of FEI, SSCS/IEEE South Brazil chapter, Cadence, OKK/Tektronix and Keysight.

We also would like to express our gratitude to all invited speakers and authors, as well as reviewers in 2024.

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Thursday, April, 18th, 2024:	**https://www.youtube.com/watch?v=fJCRFu53lw8**
09:00-10:00	**IEEE EDS– Distinguished Lecturer Presentation** **Advanced Semiconductor Technology and Device Architectures for the Next Decade.** Cor Claeys, ClaRoo, Belgium Chair: João Antonio Martino (USP)
10:00-10:30	**Coffee Break**
10:30-11:20	**IEEE EDS – Distinguished Lecturer Presentation** **Modeling FinFETs, Nanowires and Nanosheets** Antonio Cerdeira Altuzarra, Center of Research and Advanced Studies, Mexico. Chair: Marcelo Antonio Pavanello (FEI)
11:20-12:10	**IEEE EDS – Distinguished Lecturer Presentation** **2D semiconductor FET transistors: Characteristics, fabrication and modelling** Magali Estrada, Center of Research and Advanced Studies, Mexico. Chair: Marcelo Antonio Pavanello (FEI)
12:10-14:00	**Lunch**
14:00-14:30	**Opening Session**
14:30-15:30	**Painel: Política de Semicondutores do Governo Federal** Alessandro Augusto Nunes Campos – Coord. Geral de Tecnologias em Semicondutores Chair: Nilton Morimoto (USP)
15:30-15:50	**NAMITEC** Jacobus Swarts (UNICAMP) Chair: João Antonio Martino (USP)
16:00-17:50	**Poster Session 1 and Coffee** Chair: Ricardo Cardoso Rangel (USP) **Flash Presentation (2 minutes each poster) - Poster Presentation**

Friday, April 19th, 2024:	**https://www.youtube.com/watch?v=hF5C9aruwj8**
09:10-10:00	**IEEE EDS – Distinguished Lecturer Presentation** **Novel Applications of 2D Materials from AI/Memory Devices to 6G Switches to Wearable Sensors** Deji Akinwande, University of Texas – Austin, USA Chair: José Alexandre Diniz (UNICAMP)
10:00-10:30	**Coffee Break**
10:30-11:20	**IEEE EDS – Distinguished Lecturer Presentation** **Recent Applications of the Lambert's W function to device modeling** Adelmo Ortiz-Conde, Universidad Simón Bolívar, Venezuela Chair: Paula Ghedini Der Agopian (UNESP)
11:20-12:10	**IEEE SSCS– Distinguished Lecturer Presentation** **3D millimeter-wave imaging and sensing with Si-based phased arrays, edge computing, and AI** Alberto Valdes Garcia, IBM, USA Chair: Wilhelmus Van Noije (USP)
12:10-14:00	**Lunch**
14:00-15:00	**MESA REDONDA: Ensino de microeletrônica no Brasil** Chair: João Antonio Martino (USP)
INDUSTRIAL PRESENTATIONS	Chair: Paula Ghedini Der Agopian (UNESP)
15:00-15:20	**CADENCE Talk - Computational Software for Intelligent System Design** Speaker: Lucas Gaia de Castro, Engenheiro de Validação, Cadence
15:20-15:40	**OKK/TEKTRONIX Talk – Componentes SiC/GaN: 5 testes principais** Speaker: Rodrigo Schneiater – Gerente de Conta das Tektronix Brasil
15:40-16:00	**KEYSIGHT Talk** Speaker: Vitor Oliveira – Engenheiro de Aplicações da Keysight
16:00-17:50	**Poster Session 2 and Coffee** Chair: Vanessa Cristina Pereira da Silva (UNESP) **Flash Presentation (2 minutes each poster) - Poster Presentation**

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9	SF6 and C4F8 plasma for ICP/RIE SiC Etching	Rodrigo Cesar
12	Influence of Substrate doping in Floating gate MOSFET	Henrique Carvalho
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16	Schottky barrier height modulation in strained p-type silicon thin films	Paulo Gonçalves Serra Neto
17	Characterization of Switching Properties of ReRAM Devices by the Capacitance Measurements	Fernando Costa
20	A comparative analysis of Bulk ISFET and BESOI ISFET sensitivities	Pedro Henrique Duarte
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13	Characterization of MOS Capacitors on 4H Silicon Carbide Substrate submitted to ionizing radiation.	Eloi Magalhães
18	An Internal Clock Family into Low-Cost Cyclone V FPGA for High-Range and High-Resolution TDCs	Wellington Melo
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Advanced Semiconductor Technology and Device Architectures for the Next Decade

Prof. Dr. Cor Claeys

Fellow IEEE, Fellow ECS, Distinguished Lecturer IEEE EDS, Leuven, Belgium

Abstract

Semiconductor technology has known an exponential evolution in the last decades and is fully integrated in our everyday life. This necessitates implementation of novel materials, advanced design concepts and new transistor structures. Increased device performance and reduced power consumption, while maintaining a good manufacturability and yield performance without penalizing the cost/function, are driving microelectronic research towards 2-nm technologies. Device architectures such as FinFETs, TFETs, negative capacitance, Gate-All-Around, nanowires (NWs), nanosheets (NSs), CFET and Forksheet structures for logic and analog/RF building blocks enable System-on-Chip (SoC) applications. The strong progress achieved in silicon technology and heterogenous integration of Ge and III-V technologies on a silicon platform results in the on-chip integration of building blocks with different functionality. GaN offers unique features for RF applications used in base stations for mobile communication, complementing the performance of Si devices suffering from limited output power. A main challenge related to the hetero epitaxy of III-V materials on a Si substrate is the control of extended defects. There is a commercial breakthrough of GaN devices, although dependent on the application there is a competition with SiC. Major trends in process integration approaches are reviewed and technological challenges of some process modules and device structures highlighted.

Recent Applications of the Lambert's W function to device modeling

Prof. Dr. Adelmo Ortiz-Conde

Solid State Electronics Laboratory, Simón Bolívar University, Caracas, Venezuela

Abstract

We present a review of recent uses of the special mathematical function known as the Lambert's function for device modeling applications. The nowadays ubiquitous W is a multivalued special mathematical function implicitly defined as the inverse function of the linear-exponential transcendental equation , which can be solved for only when , where k represents the branch number. W was originally formulated by Leonhard Euler in 1783, and revived by Edward M. Wright in 1959 and later rescued for practical use in 1996 by Robert M. Corless and coworkers. The W function's name "Lambert" commemorates Johann Heinrich Lambert's Transcendental Equation of 1758, and the use of the symbol "W" acknowledges the pioneering work of Wright on the subject. As far as we know, the first application of Lambert's function to device modelling was proposed in 2000 by Banwell, specifically for the case of a diode with parasitic series resistance. Three years later in 2003, the W function was again used in electronics for the first time for MOSFET modeling, originally for explicitly describing the channel surface potential of undoped channel MOSFETs. The W function continued to be used in a growing number of occasions and situations related to MOSFET modeling. Among the many instances W has been used ever since for this purpose are: ultrathin body nanoscale devices, Double Gate and Surrounding Gate devices, polySi thin film transistors (TFTs), undoped and lightly- doped symmetric Double Gate devices, GAA undoped polySi nanowire devices, for FDSOI MOSFET parameter extraction, for charge and capacitance modeling in tunnel FETs, MOSFET modeling at deep cryogenic temperatures], in the Generalized EKV Compact MOSFET Model], to describe the charge density in Transition Metal Dichalcogenide FETs, and lately also for nanosheet transistors.

Novel Applications of 2D Materials from AI/Memory Devices to 6G Switches to Wearable Sensors

Prof. Dr. Deji Akinwande

University of Texas – Austin

Abstract

This talk will present our latest research adventures on 2D nanomaterials towards greater scientific understanding and advanced engineering applications. In particular, the talk will highlight our work on flexible electronics, zero-power devices, single-atom monolayer memory, non-volatile RF/5G/6G switches, and wearable tattoo sensors for mobile health. Non-volatile memory devices based on 2D materials are an application of defects and is a rapidly advancing field with rich physics that can be attributed to metal adsorption into vacancies. The memory devices can be used for neuromorphic computing and operate as switches up to 500GHz. Likewise, from a practical point, electronic tattoos based on graphene have ushered a new material platform that has highly desirable practical attributes including optical transparency, mechanical imperceptibility, and is the thinnest conductive electrode sensor that can be integrated on skin for physiological measurements including blood pressure monitoring. Much of these research achievements have been published in leading journals.

Modeling FinFETs, Nanowires and Nanosheets

Prof. Dr. Antonio Cerdeira Altuzarra

Solid State Electronics Section, Dep. of Electrical Engineering, Center of Research and Advanced Studies, Mexico City, Mexico

Abstract

The transition from two-dimensional (2D) transistors to three-dimensional (3D) transistors at the beginning of the 21st century required the development of new models for 3D transistors. The work of developing models of semiconductor devices is a typical activity of the Academy, which our group followed, beginning the development of a new model for 3D FinFET devices, in 2006. These devices have a silicon fin, surrounded by three gates, two laterals and one on the top. The Si layer is narrow enough, creating a potential distribution across its thickness, where the potential at the center is different from zero. Considering this potential distribution and the fact that the Si layer is doped, lead to a transcendental equation for the distribution of the electric field from gate to gate, that has no direct analytical solution. In this presentation we will show an example of a compact, continuous and analytical model known as Symmetric Doped Double-Gate Model (SDDGM), where the indicate problems were solved. The model was complemented with variable mobility, the effects of short channel, leakage currents and dependence on ambient temperature. In addition, it was demonstrated that this model can be used to model also recent 3D structures, such as nanowires, nanosheets and stacked nanosheets. Validation of the using this model for these new devices will be shown. SDDGM was implemented in the circuit simulator SmartSPICE, using Verilog-A language. Even today, the development of more precise models, as well as complements for applying them to new devices, is an open topic for the Academy.

2D semiconductor FET transistors: Characteristics, fabrication and modelling

Profa. Dra. Magali Estrada

Solid State Electronics Section, Dep. of Electrical Engineering, Center of Research and Advanced Studies, Mexico City, Mexico

Abstract

The metal-oxide-semiconductor field effect transistor, where silicon is the semiconductor material, Si MOSFETs, and their successors FINFETs and multigates devices (nanowires, nanosheets, stacked devices, etc) are at present, the basic semiconductor device allowing the tremendous development reached by actual semiconductor industry to meet the requirements of data processing, artificial intelligence mobile devices and other techniques necessary for economic, social, and scientific development. To achieve the required demands, it has been necessary a constant reduction of the transistor size, which has the prediction of Moore´s Law, of duplicating the number of transistors in a chip every two-three year. This miniaturization process has had to overcome important problems related to parasitic effects present in bulk materials called short channel effects (SCEs). For example, as the channel length is reduced, the device current in the below threshold regime will increase, and so, the static power consumed. A detailed study of the electrostatic characteristics of FET devices, described by Poisson equation can be done, using the so-called characteristic channel length, defined as , where xs and xi are the width and thickness of the semiconductor layer and insulator, respectively, and ks, ki, their relative dielectric constants. λ can be reduced, by reducing the thickness of the semiconductor or the insulator layers, as well as, by increasing the relative dielectric constant of the insulator layer. However, in bulk 3D semiconductors, the reduction of xs, increases the threshold voltage VT., due to the increase of defects as dangling bonds and interface states at the interface of the semiconductor/dielectric. At the same time, mobility decreases as xs6 due to the increase in carrier scattering at the surface. In general, for ultrathin 3D FETs, the electrostatic control of carriers in the channel is reduced, while the leakage current increases. On the contrary, in a two-dimensional (2D) material, electrons can be naturally confined within a very thin channel formed by few monoatomic layers, where carriers can in principle uniformly controlled by the gate voltage, while the leakage current reduces. For the above reasons, during the last years, much work has been done regarding the possibility of using 2D semiconductors to overcome the above-mentioned limitations in further scaling of 3D semiconductor devices. In this talk, we will analyse some of these characteristics, as well as results obtained in fabricating 2D semiconductor FETs, using different methods. Finally, we will present some work done on modelling these new devices, already available and discuss challenges to overcome.

3D millimeter-wave imaging and sensing with Si-based phased arrays, edge computing, and AI

Dr. Alberto Valdes Garcia

IBM Thomas J. Watson Research Center, USA

Abstract

The use of millimeter-wave frequencies for 5G networks has been a primary contributor for transitioning Si-based phased array technology from R&D to real-world deployments. While the commercial use of millimeter-wave sensing so far has been dominated by low- cost, compact MIMO radars for automotive and industrial applications, the on-going wide deployment and advancement of Si-based phased arrays opens a new horizon of opportunities for sensing and event recognition. This talk will first cover the fundamentals and KPIs of 3D radar systems using phased arrays including associated key circuit design and packaging design techniques. Examples of such 3D radar systems at 28-GHz, 60-GHz and 94-GHz will be provided. Next, the presentation will describe how the full potential of such systems can be realized through synergistic co-design with algorithms and edge computing assets. Key examples of emerging applications based on these vertically integrated antennas-to-software/AI systems will be provided including multi- spectral imaging, 5G mmWave joint sensing and communications, and AI-based recognition of human gestures and concealed objects.

Materials Applied to Rectangular Dielectric Resonator Antenna (RDRA) Targeting 5G Applications

Marcos G. F. dos Santos[1], Igor R. S. Miranda[2], Fiterlinge M. Sousa[1], Fabio B. de Sousa[1,3] and Marcos B. C. Costa[1]

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1. Abstract

This study conducts a dual assessment, employing two commercial software applications, of a model of RDRA operating at a central frequency of 28 GHz, targeting 5G applications. The simulated materials consist of Ceramic Alumina (Al_2O_3) and a Low-Temperature Co-Fired Ceramic (LTCC) LMP-CTO-KMO. The antennas with LMP-CTO-KMO resonators showed the most promising results, achieving an (S_{11}) value of -43.67 dB at 28.6 GHz, a bandwidth of 2670 MHz, and a gain of 6.5 dB.

2. Introduction

Currently, with the proliferation of interconnected devices in the Internet of Things (IoT) context, the number of connections has exponentially increased, imposing a growing demand for quick and instantaneous responses. [1] Dielectric Resonator Antennas (DRA) have stood out as one of the most promising options for 5G applications in mobile devices. They offer compactness, wide bandwidth, and miniaturization proportional to $\lambda_0/\sqrt{\varepsilon_r}$. The use of dielectric materials as resonators dates back to 1938, with Richtmeyer's contributions [2]. Materials with high permittivity ($\varepsilon_r > 20$) are particularly advantageous for these applications [3]. In recent decades, there has been significant research focus on this type of material, that has high permittivity (ε_r) for use as component of antenna.

This work proposes the simulation and design of rectangular geometry Dielectric Resonator Antennas (DRA). These simulations aim to investigate the behavior of materials with ε_r in the range of 9 to 30. The feeding technique employed is the slot method, resulting in resonance frequency range of 28 GHz, aligned with 5G applications.

3. Simulation Model

Rectangular Dielectric Resonator Antennas consist of a rectangular dielectric resonator positioned on a square substrate and a metallic ground plane. Figure 1 illustrates the design of the proposed project. The antennas were designed to operate with Rogers Duroid 5880 substrate. Rectangular resonator antennas are calculated through the transcendental equation (1), which has equation (2) as its solution [3]:

$$tan(k_z d) = \frac{k_z}{\sqrt{(\varepsilon_r - 1){k_0}^2 - {k_z}^2}} \quad (1)$$

$$\varepsilon_r {k_0}^2 = {k_x}^2 + {k_y}^2 + {k_z}^2 \quad (2)$$

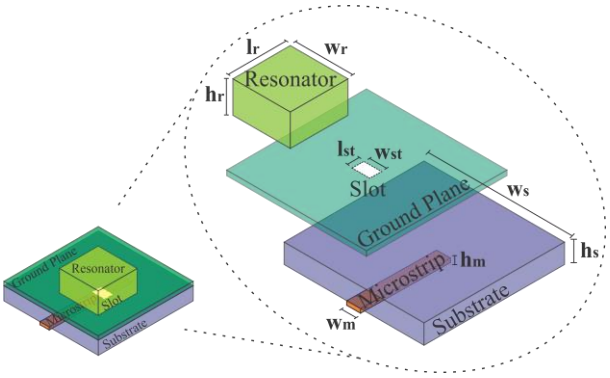

Fig.1. *Antenna Design*

Table 1 presents the parameters used for the DRA model, where w is width, l is length and h is height, followed by the initial of each component.

Table I. *Antenna Parameters (mm)*

Sim's	$l_r \times w_r \times h_r$	$w_s \times h_s$	w_m	l_{st}	w_{st}
01	3.4 × 2.102 × 1.0171	9.9 × 0.254	0.73	1.72	0.67
02	3.4 × 1.3 × 1.5	9.9 × 0.254	0.73	1.82	0.23

4. Materials

The materials employed were alumina (Al_2O_3) ε_r of 9.8 with a purity of at least 99%, readily available in the software library (Simulation 01) and LTCC (Low-Temperature Co-Fired Ceramic) phosphate LMP-CTO-KMO doped with molybdenum, ε_r of 9.1 [4], referred to as LMP (Simulation 02).

5. Results and Discussion

Comparing the results, in the HFSS software, simulation 01 exhibits a higher (S_{11}) coefficient. However, in both software, simulation 02 showed a wider bandwidth, approximately 42% larger compared

to simulation 01. Both simulations resonate near the central frequency of 28 GHz.

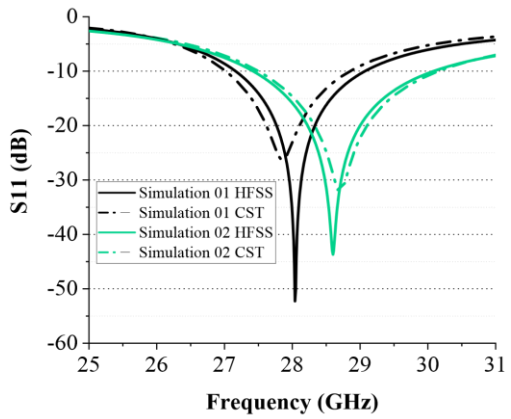

Fig.2. *S_{11} parameter's simulations.*

When observing the variation in results due to the use of HFSS and CST software, where no significant discrepancy is noted, one can overlook such relatively small variations and attribute them to the different approaches of the methods as well as variations in modeling.

Table II. *Simulation's Results*

Simulation	Freq. (GHz)	BW (MHz)	Gain (dB)	VSWR
01 HFSS	28.06	1880	6.1	1.04
02 HFSS	28.6	2670	6.5	1,38
01 CST	27.85	1856	5.78	1.10
02 CST	28.7	2650	6.16	1.04

Figure 3 shows the 2D radiation pattern with a gain of 6.5 dB in the maximum direction and 3D radiation pattern, both for the LMP antenna simulation in HFSS, in CST the lobules have the same display.

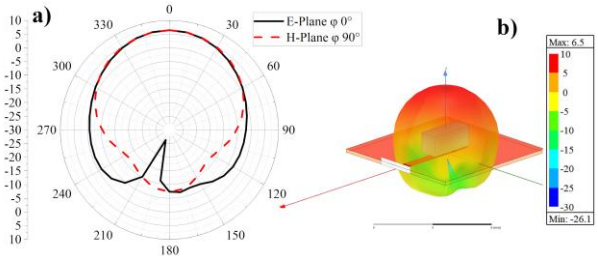

Fig.3. *a) 2D gain radiation pattern of LMP. b) 3D radiation pattern of LMP.*

The simulations proposed in this work investigate the effectiveness of ceramic materials as resonators for DRA antennas.

Barman and Dasgupta [5] designed a DRA with a resonator material ($\varepsilon_r = 10$) for 5G. This study simulations shows that gain values of simulation 02's are preferable. Additionally, the total volume is reduced, and the geometries are simplified.

Table III. *Comparison with the literature*

Material	Freq. (GHz)	ε_r	BW (MHz)	Gain (dB)	Ref.
Rogers RT	28	10.2	2800	6.17	[5]
-	28.08	3.0	3776	7.12	[6]
Al_2O_3	28.06	9.8	1880	6.1	This study
LMP	28.6	9.1	2670	6.5	This study

6. Conclusions

Simulation 02 demonstrating superior characteristics, including a 42% wider bandwidth, higher gain, and reduced size. The simulated models showed maximum energy transfer, reduced reflection and noise. The material LMP-CTO-KMO, used as the resonator in simulation 02, consistently exhibited superior properties. Consequently, LMP-CTO-KMO emerges as a highly viable material for a wide range of applications, including 5G technology, microwave technology, and MIMO antennas. Alumina presents itself as a good candidate when considering the ease and feasibility of its application, being a ceramic material with excellent thermal and dielectric properties.

Acknowledgments

This study was financed in part by the Coordenação de Aperfeiçoamento de Pessoal de Nível Superior - Brasil (CAPES) - Finance Code 001.

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Study of a Two-Dimensional Photonic Crystal Demultiplexer based on Graphene

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1. Abstract

In the present work, an eight-channel 2D photonic crystal demultiplexer based on graphene is presented for application in optical systems that use the wavelength division multiplexing (WDM) technique. The photonic device was designed based on a square crystalline lattice of silicon dielectric rods immersed in air and is formed by three main parts: Bus waveguide; Resonator rings and L-curved waveguides. COMSOL multiphysics Software was used to study and simulate the designed structure. In analyzing the simulation results, the resonant wavelength, spectral width, Quality factor, Transmission efficiency and channel spacing were evaluated for the demultiplexer's eight transmission channels. In general, the values for the analyzed parameters proved to be considerable regarding the application of the photonic device in optical wavelength division multiplexing (WDM) systems.

2. Introduction

Over the past few decades, the relentless endeavor to enhance and innovate in optical communication technologies has steered research towards new horizons, such as the exploration and application of alternative materials in the development of more effective and compact systems. Among these materials, notable examples include photonic crystals and graphene.

Photonic crystals are structures that manipulate light through periodic variation of the dielectric constant, creating photonic band gaps for electromagnetic propagation. The modeling of these structures allows precise control of light, being useful in optimizing optical communication systems and miniaturizing integrated circuits[1].

Graphene, in turn, is a two-dimensional material made from a single layer of carbon atoms, arranged in hexagonal structures. Its atomic bonds give it excellent mechanical, electronic and optical properties, making it versatile in various applications[2].

In this regard, the present study investigates a two-dimensional photonic crystal demultiplexer based on graphene for application in systems employing the Wavelength Division Multiplexing (WDM) technique. The article is organized as follows: The materials and methods are discussed in the third section, the results and discussions in the fourth, and finally, the conclusions and references.

3. Materials and Methods

In the simulations, the Finite Element Method (FEM) was used, using the COMSOL Multiphysics software, where the transmission parameters of the designed demultiplexer were analyzed.

A. Graphene Conductivity

Graphene was modeled based on its local surface conductivity, considering the intraband contribution given by the Drude model [3]:

$$\sigma(\omega) = \frac{2e^2}{\pi\hbar}\frac{k_B T}{\hbar}\ln[2\cosh(\frac{\mu_c}{2k_B T})]\frac{i}{(\omega + i\tau^{-1})}\ , \quad (1)$$

and interband contribution given by

$$\sigma_i(\omega) = \frac{e^2}{4\hbar}[H(\frac{\omega}{2}) + i\frac{4\omega}{\pi}\int_0^\infty \frac{H(\varepsilon) - H(\frac{\omega}{2})}{(\omega^2 - 4\varepsilon^2)}\, d\varepsilon]. \quad (2)$$

Where $\tau = 10^{-13}$ is the graphene relaxation time, T is the temperature and μ_c is the chemical potential.

B. Photonic device structure

The structure of the proposed photonic crystal demultiplexer was based on works [4, 5], which consists of three regions: Bus waveguide; Resonator rings; and L-curve waveguides, as shown in Fig. 1.

The resonator rings have octagonal geometry, the graphene is located in the selector rods inside the L-curved waveguides and the three regions are interconnected through coupling rods. Additionally, the device operates with a bandgap in the range of $0.30 < a/r < 0.44$ for transverse magnetic (TM) polarization, and its construction was achieved by introducing defects and varying the geometric parameters of a two-dimensional square lattice of silicon dielectric rods ($n_{Si} = 11.90$)

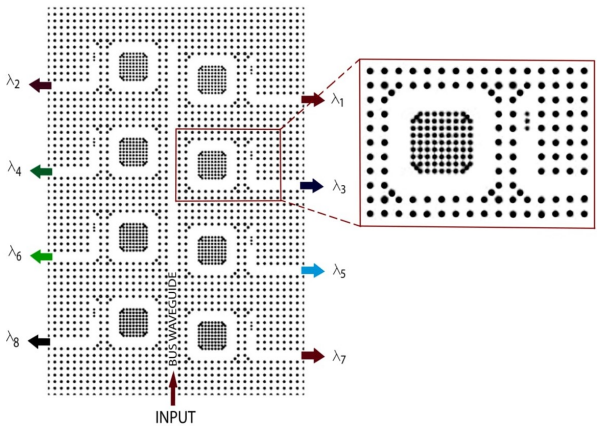

Fig. 1: Geometry of 2D photonic crystal demultiplexer with graphene.

immersed in air ($n_{air} = 1.0$), with dimensions of 40 x 60, rod radius $r = 100$ nm, and lattice constant $a = 560$ nm [6].

4. Results and Discussion

Figure 2 presents the normalized transmission spectra for the output channels of the designed demultiplexer.

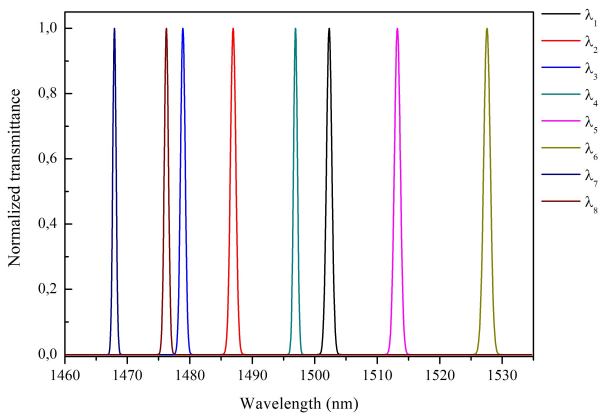

Fig. 2: Transmission spectra at simulated demultiplexer outputs.

The simulation analyzes show considerable values for the transmission efficiency of the demultiplexer's eight channels, averaging around 90.62 %. The λ_1 channel, for example, operates with a resonant wavelength (λ) of 1,502.31 nm, Spectral width ($\Delta\lambda$) of 1.00 nm, quality factor Q equal at 1,502.31 and transmission efficiency 93.63 %.

Figure 3 shows the electric field distribution for the λ_1 channel. In practical terms, the multiplexed signal enters through the bus waveguide, part of this signal is coupled to the resonant ring which is then directed to the L-curved waveguide. graphene operate by improving the transmission efficiency of the wavelength transmitted by the output channel.

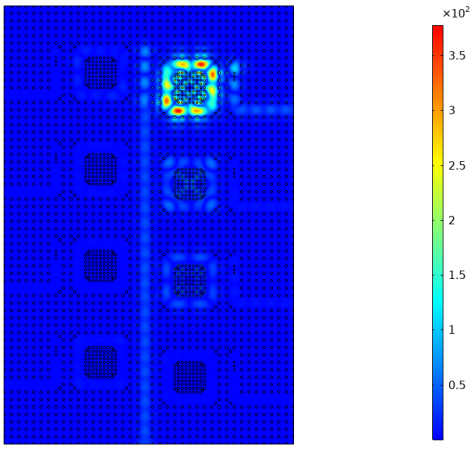

Fig. 3: Electric field distribution for λ_1

5. Conclusions

In this work, a graphene-based 2D photonic crystal demultiplexer was proposed. The device was simulated and studied using COMSOL Multiphysics software. And the results obtained for the device's transmission parameters proved to be considerable for its application in WDM systems.

Acknowledgements

This study was financed by the Conselho Nacional de Desenvolvimento Científico e Tecnológico - Brasil (CNPq).

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SF_6/O_2 and C_4F_8 plasma for ICP/RIE SiC Etching

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1. Abstract

In this study, ICP/RIE plasma was employed to etch the SiC substrate. Two different gas combinations were utilized: SF_6/O_2 gas combination in one sample, and C_4F_8 in another sample. Scanning electron microscopy (SEM) was utilized to examine the angle and structure of the etched SiC wall, as well as to observe any particulates present after etching. The SF_6 plasma exhibited less particulate formation when connecting the wall with the substrate at an angle close to 90º. Conversely, the C4F8 plasma demonstrated a higher corrosion rate, more particulates, and a rounded angle between the wall and substrate.

2. Introduction

Silicon carbide (SiC) has become a very promising material in the microelectronics industry due to its properties such as: high thermal conductivity, high breakdown voltage (3.8×10^6 V/cm), high mechanical hardness, high band gap (greater than 2.4 eV), good chemical stability, high electron saturation speed (approximately 2×10^7 cm/s) and high thermal conductivity [1]. Therefore, it is ideal for developing devices that can be used in extreme power and temperature conditions, for example, in satellites, nuclear reactors and the aeronautical industry in general [1].

Very-large-scale integration (VLSI) is a process that integrates millions of MOS transistors, diodes, capacitors, and other passive components onto a single chip [2]. Consequently, it is essential to isolate these devices from each other. One method to achieve this is by corroding the boundaries of each device, penetrating the substrate, and effectively isolating them from one another. [2-7].

Therefore, this study focuses on investigating the use of ICP/RIE plasma to etch the SiC substrate. Two different gas combinations were employed: SF_6/O_2 gas combination in one sample, and C_4F_8 gas in another sample. Scanning electron microscopy (SEM) was utilized to observe the angle and structure of the etched SiC wall, as well as to determine the presence of any particulates after etching.

3. Material and Methods

N-Type <001> SiC samples were employed in this study. Initially, RCA cleaning was performed on the samples. Next, the lithography process was carried out to create grid structures for observing the corroded SiC wall. Following lithography, aluminum was deposited to serve as a hard-mask. Table 1 presents the parameters of the two recipes used to etch SiC.

Table I. *Recipes used for SiC etching in sample 1 (SF_6/O_2) and 2 (C_4F_8).*

Parameters	Sample 1	Sample 2
RIE	200W	50W
ICP	1200W	1000W
Flow C_4F_8	100sccm	-
Flow SF_6	-	20sccm
Flow O_2	-	5sccm
Flow Ar	5sccm	-
Pressure	45mTorr	45mTorr
DC Bias.	606V	150V
Time	15min	5min

The corrosion process involved utilizing the Plasmalab System 100 from Oxford Instruments. SEM analysis was conducted to observe the quality of the wall, the quantity of products/dirt generated by corrosion, and to analyze the angle formed between the wall and the floor. For this purpose, a SEM FEG Mira 3 XMU-TescanX was employed. The height of the wall was determined using the Burke profilometer.

3. Results and discussion

A. Sample 1 - C_4F_8 plasma.

Fig.1 shows the SEM images of the C_4F_8 plasma etched samples. In this Fig., it is evident that there are particulates present, noticeable both on the Al film and on the SiC substrate (Fig. 1A and B). Fig. 1B demonstrates that these particles vary in size. Additionally, Fig. 1C reveals that the connection between the end of the wall and the substrate exhibits a rounded shape. This rounding is favorable, as 90º angles can act as antennas, potentially degrading the device and electrical measurements. Through profilometry, it was determined that the substrate corrosion depth was 1.6 microns. Comparing this result with the literature, which employs C_4F_8 plasma, it becomes apparent that this study

achieved a higher corrosion rate than those reported [5,6]. However, further refinement of the recipe is necessary to minimize particulate formation.

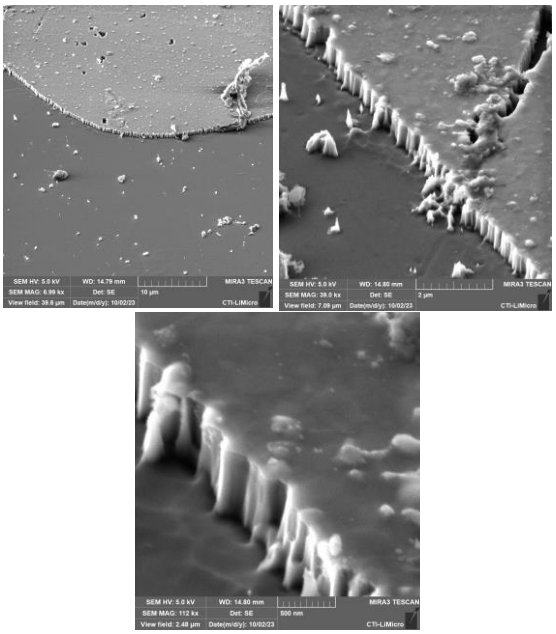

Fig.1. *SEM image of sample 1, scale of; A) 10um, B) 2 um and C) 500nm.*

B. Sampe 2 - SF_6/O_2 *plasma.*

Fig. 2 shows SEM images of the SF_6/O_2 plasma etched samples, revealing the presence of small particles on both the Al film and the SiC substrate (Fig. 2A and B). However, these particulates appear to be smaller compared to those generated by C_4F_8 plasma.

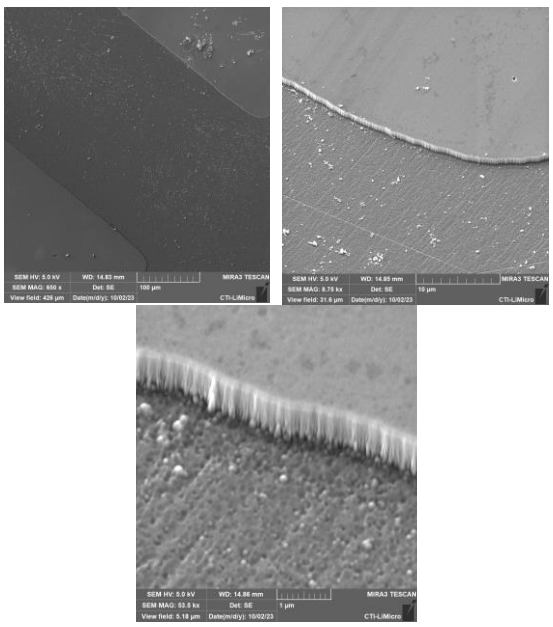

Fig.2. *SEM image of sample 1, scale of; A) 10um, B) 2 um and C) 1um.*

Additionally, the connection between the wall and the substrate exhibits a less rounded shape, closer to a 90º angle, compared to the C_4F_8 plasma etching. This angular configuration is undesirable, as mentioned in the previous analysis. Profilometry analysis determined that the substrate corrosion depth was 1 micron. Although this corrosion rate is lower than that obtained for C_4F_8 plasma, it resulted in less particulate formation. Moreover, it is comparable to the corrosion rate reported in the literature for plasma etching with the same gas combination and flow values [3-5]. However, it was expected that the shape of the connection between the wall and the substrate would be rounded.

4. Conclusions

With these preliminary results we can conclude that the two plasmas present good corrosion rates on 1 micron SiC.

The SF_6/O_2 plasma showed little particulate matter, a lower rate compared to C_4F_8, and an angle between wall and substrate close to 90º.

The C_4F_8 plasma showed a higher corrosion rate than the SF_6/O_2 plasma, with a lot of particulates of different sizes but an angle between the wall and the rounded substrate.

However, it is worth highlighting that more testing and refining the recipes are necessary.

Acknowledgments

Authors would like to thank CCSNano staff for help in sample preparation and processing. This work was supported by ROTA 2030, grants number [28795-23].

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Influence of Substrate doping in Floating gate MOSFET

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1. Abstract

The work demonstrates the operation of the Floating-Gate MOSFET and presents the behaviour of a 6nm thick Silicon <100> Floating-Gate MOSFET with tunnelling and a top gate oxide made of SiO2 with 6nm thickness, employing LDD technology. It also discusses the influence of substrate doping on the device between 10^{15} and 5.10^{18}.

2. Introduction

The Moore's Law has led to rapid advancements in micro and nanoelectronics, resulting in decades of size reduction in semiconductor device and increased density, causing significant societal changes. Additionally, there has been a trend of decreasing energy consumption and manufacturing costs over time [1-2]. Among various electronic devices, one of the main ones include logic devices and memories, which dominate the large market share. Over the years, the Floating-Gate MOS transistor (FGMOSFET) has garnered attention due to its properties, such as compatibility with MOS manufacturing processes, integration into mixed-signal integrated circuit designs, and its impact as a high-density, high-speed, and low-power non-volatile memory [3,4,5].

The use of a floating gate as a charge-trapping layer is widely employed in Flash memories, based on a simple single-transistor device structure, enabling higher integration density compared to other memory devices [1]. However, there are technological challenges related about limit of tunnel oxide thickness. When the thickness is too thin (less than 6 nm), charge leakage stored in the floating gate becomes substantial, increasing energy dissipation and degrading charge retention time and memory window performance [6,7].

3. Devices characteristics and operations

A. Characteristics

The simulated device studied in this work is an n-type FGMOSFET, as showed in Fig. 1 (a), with silicon <100> floating gate of 6nm thickness. It features a top gate and tunneling oxide made of SiO2 with a thickness of 6 nm, LDD with an Arsenic concentration of 3.10^{18}, a channel length of 0.1 µm, and source-drain with an Arsenic concentration of 10^{19}. Additionally, it has a metal gate made of polysilicon.

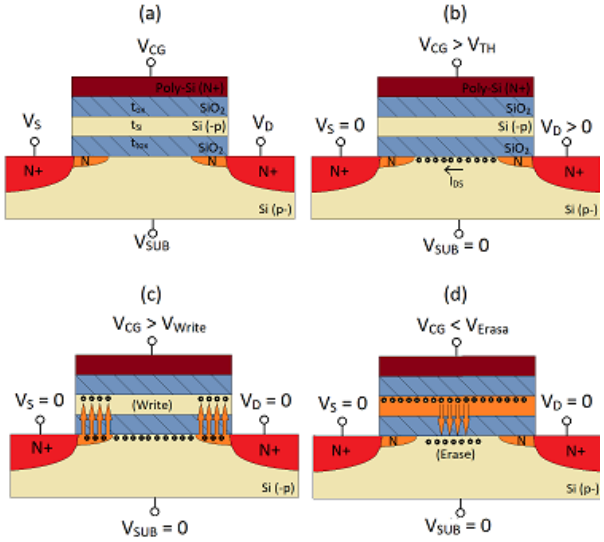

Fig.1. *n-type FGMOSFET (a), read (b), write (c) and erase (d) operations.*

B. Write, Erase and Read Operations.

Initially, there is no stored charge on the floating gate ($Q_{FG} = 0$). By applying voltage to the control gate ($V_{CG} = V_{Th}$), electrons move from the substrate to the oxide interface, creating a channel as shown in Fig. 1 (b) (c). Increasing applied voltage (V_{write}) , the Fowler-Nordheim tunneling mechanism transports charge to the floating gate, making $Q_{FG} < 0$ (Fig. 1 (c)). When the applied voltage is removed, the charge is trapped in the floating gate. This mode of operation is defined as the "write" operation. The erase operation has the opposite goal, aiming to remove the stored charge. For this, a negative voltage is applied to the control gate ($V_{CG} \leq V_{erase}$), as depicted in Fig. 1 (d). Thus, the transistor's threshold voltage is given by equation (1).

$$V_{Th} = V_{FB} + 2\Phi_{fp} + Q_{FG}/C_{CG} \quad (1)$$

Where V_{FB} and Φ_{fp} are the flat-band potential and Fermi potential, respectively. Thus, (2) give the shift in the threshold voltage of the Floating-Gate MOSFET transistor or memory window.

$$\Delta V_{Th} = V_{Th} - V_{Th0} = -Q_{FG}/C_{CG} \quad (2)$$

Where V_{Th0} and V_{Th1} are the threshold voltages before and after charge injection into the floating gate (erased and writen operation), respectively.

4. Results and discussion

The Fig. 2 show the space charge in floating gate in function of time for writing (V_{CG} = 12 V), retention (V_{CG} = 0 V), and erase (V_{CG} = -12 V) operations. It is observed that during the writing operation, there is an accumulation of electrons in the floating gate due to the Fowler-Nordheim tunneling mechanism. After the writing process, when V_{CG} became 0, the floating gate charge is trapped in the region due to the isolation of the tunneling and top oxide. In the erase operation, defined by V_{CG} = -12 V, the stored charge in the floating gate is removed, returning Q_{FG} to approximately 0.

The Fig. 3 presents the drain current in a function of the control gate voltage after the write and erase processes. It is evident that the accumulation of stored charge in the floating gate causes a shift in the transistor's threshold voltage, as described by equation (2), and this difference is defined as the memory window.

However, the memory window region can be adjusted by tuning the substrate doping in the manufacturing process to reduce power dissipation, as shown in Fig. 4. Therefore, it becomes interesting to design a device using low substrate doping, as the memory window is not influenced by substrate doping.

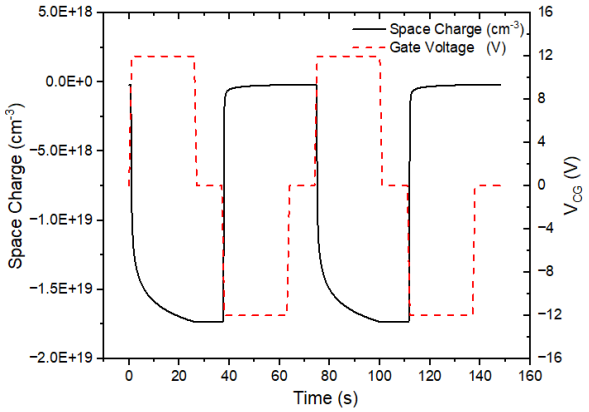

Fig.2. *Space charge in floating gate in function of time, for written, retention and erase operation.*

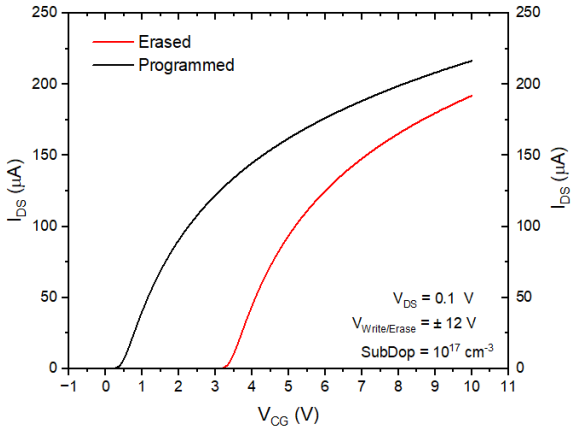

Fig.3. *Drain current read in function of control gate voltage, after write and erase operations.*

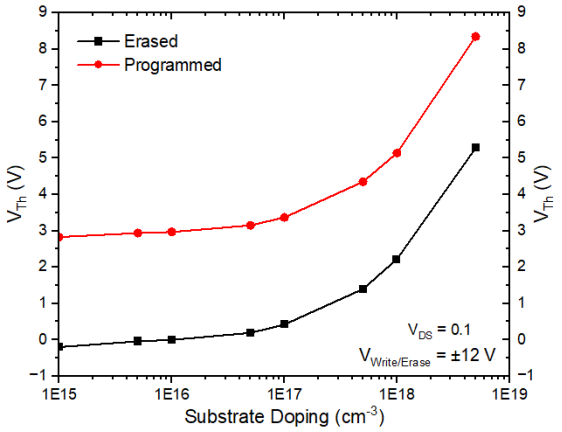

Fig.4. *Threshold voltage in function of substrate doping in n-type FGMOSFET, for write and erase operations*

5. Conclusion

In conclusion, the study of the n-type FGMOSFET device revealed the dynamic behaviour of the charge on the floating gate during write, retention, and erase operations. The accumulation and removal of charge were observed, demonstrating the Fowler-Nordheim tunnelling mechanism. The variation of drain current with control gate voltage creating a memory window with the erase and programming operation is essential for the device's operation as a non-volatile memory. Furthermore, the ability to adjust the memory window through control of substrate doping between 10^{15} and 5.10^{18} presents a promising strategy to optimize device performance, reducing energy dissipation. The design with low substrate doping proved particularly advantageous, as the memory window remained robust and minimally influenced by substrate doping in threshold voltage. These insights contribute to enhancing the efficiency and reliability of FGMOSFET de, fostering advancements in high-density non-volatile memories.

Acknowledgments

The authors would like to thank CAPES and CNPq for the financial support.

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Investigation of a Three-Ring Coupled Photonic Molecule for Enhanced Refractive Index Sensing Applications

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1. Abstract

Photonic devices that use ring-shaped resonant cavities have the ability to control energy in the form of light, which has several applications, including high sensitivity in refractive index (RI) detection. The coupling of these cavities to create an architecture with two or more rings, known as Photonic Molecule (PM), makes it possible to design the spectral response of new devices based on these PMs, directing them towards certain applications. This work investigates a PM architecture for application as a RI sensor. To ensure light-analyte interaction, we demonstrated the use of a detection window capable of exposing the surface of the PM's embedded rings and investigated its impact on the PM's spectral response and sensing capability.

2. Introduction

In integrated photonic devices, some elements are fundamental, such as: waveguides, optical couplers and optical cavities. Waveguides are responsible for confining light through the concept of reflection between two or more different media to work and guide the light efficiently; couplers are responsible for coupling light between device elements to propagate signals from one element to another, such as coupling between optical fibers and integrated waveguides; and optical cavities are responsible for confining photons in tiny regions, providing high power with low energy consumption. With these fundamental elements it is possible to build various types of integrated photonic devices, such as the proposed sensor in this work.

When working on projects aimed at the area of sensing using devices with resonant cavities, a necessary requirement is to ensure that the resonators have high fabrication quality, well-defined resonances and that they occupy a reduced area on the chip. This need is linked to the condition that the Quality Factor (Q), the Free Spectral Range (FSR) and the cavity radius (R) can be independent in Photonic Molecules (PM) [1]. The PM is formed through electromagnetic coupling between several ring-shaped resonators coupled in a favorable geometry and in conjunction with rectangular waveguides. When several ring-shaped resonators are coupled to form PMs, the FSR and Q do not depend exclusively on the radii of the rings but on the elaborate geometric combination, the coupling conditions and the number of rings [1,2]. The characteristics enabled by PMs, combined with their ability to confine light and interact with specific analytes, ensure their relevance for sensing applications, especially in detecting subtle variations in the refractive indices of various solutions [3].

3. Methodology

Device sensitivity simulations were conducted using the FullWave module of RSoft software.. The effective index method was used to guarantee the lowest possible computational effort [4]. To simulate the proposed sizes, external ring with radius 20μm and internal rings with radii equal to 9.4375μm were used, silicon waveguides in standard dimensions (450nm x 220nm), with wavelength varying in the infrared spectrum (1.46μm - 1.62μm). The coupling distance between the embedded rings and outer ring was 150nm and between outer ring and bus waveguide was 200nm. To guarantee the functioning of the device proposed as an RI sensor, it was proposed to open a detection window in the coupling region between the inner cavities of the device, allowing the light that propagates in these rings to interact with the analyte present there, as shown in Figure 1.

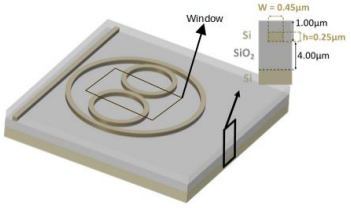

Fig.1. *Photonic device proposed in this project, with details of the SOI platform used and its dimensions.*

To simulate the presence of this window and the change in the effective index in this region, the device was simulated using the effective index method for each analyte present in the window. The materials used as analyte solutions were water or ethylene glycol (EG) diluted in water, with concentrations ranging from 5% to 25% dilution. Table 1 shows the RI values for the solutions of EG diluted in the water used. In the detection window, the region of the waveguides that form the embedded rings were considered the effective indices identified as N_{slab} in Table 1, whereas the region where

there are no rings the value of the n analyte was considered in the simulation.

Table 1. *RI of the light in the respective solutions.*

Solution	n	N_{Slab}
H_2O	1.3166	2.4669
5%EG-H_2O	1.3217	2.4677
10%EG-H_2O	1.3270	2.4684
15%EG-H_2O	1.3319	2.4691
20%EG-H_2O	1.3379	2.4700
25%EG-H_2O	1.3430	2.4707

4. Results

Simulation-generated transmission spectra of the PM, depicting varying EG concentrations in water within the detection window, are shown in Figure 1. The proposed device has the following spectrum shown in Figure 2, with the resonances of the larger external cavity represented by the larger valleys in the spectrum and the resonances of the smaller internal cavities represented by the smaller valleys. Particularly in this PM configuration, as the inner rings are coupled to each other, when their resonances are very close but far from the resonance of the outer ring, a quadruplet of resonances is predicted to appear [2]. Our proposal is to use the change in each of the resonances of this quadruplet for detection. An analysis was carried out using the conventional sensitivity calculation method, defined as [4], which takes the resonance of the larger cavity as a reference. The calculation consists of taking the distances of the quadruplet resonances of the inner rings relative to the outer ring resonance for each analyte concentration in the device window. To carry out this calculation, only a part of the spectrum was considered where the resonances of the inner rings did not interfere with those of the outer ring, that is, for a non-degenerate condition between the resonances of the internal cavities with the external cavity [2]. In Figure 2, d1, d2, d3 and d4 exemplify the distances used in calculating the sensitivity for a quadruplet in which d1, d2, d3 and d4 are the distances referring to the 1st, 2nd, 3rd and 4th valleys of the quadruplet. Figure 3 shows the displacement caused in the resonances of the inner rings by the different concentrations of EG present in the detection window.

From the deviations of the calculated resonances in relation to the RI of each analyte represented in Table I, it was possible to generate the sensitivity curves of the PM sensor. The sensitivity curves are represented in Figure 3 and there is a sensitivity curve for each resonance of the quadruplet. S1 is related to the first quadruplet resonance and so on respectively. The generated curves are linear, making it possible to calculate sensitivity using equation 1:

$$S_i = \Delta d_i / \Delta n \qquad (1)$$

which represents the angular coefficient of each curve of Fig. 3. In this equation 1, d_i represents the distance between the resonance i of the inner rings in relation to the resonance of the outer ring and n is the RI of the analyte. The highest value for sensitivity found using the conventional method was 39.77nm/RIU. When checking this fourth resonance, it has the highest Q (28,446) among the four in the quadruplet, since its resonance linewidth is smaller, a fact that explains its greater sensitivity.

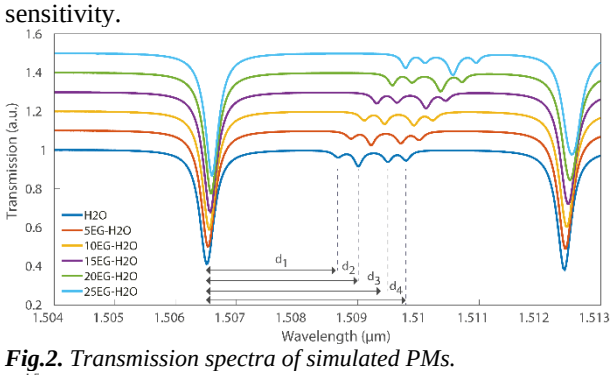

Fig.2. *Transmission spectra of simulated PMs.*

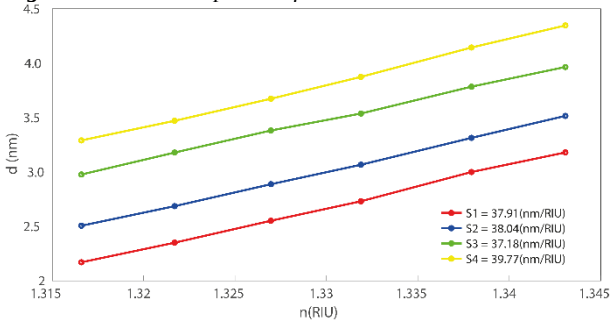

Fig.3. *Calculated sensitivity curves.*

5. Conclusions

The proposed sensor has enormous potential for use in the area of RI sensing, enabling the acquisition of four sensitivity curves within a single compact device, thereby opening up novel detection possibilities in the future. The highest sensitivity found was 39.77nm/RIU, compatible with compact refractive index sensors obtained with PMs. The authors would like to thank the UNICAMP Device Research Laboratory for their support in simulations with RSoft.

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Schottky barrier height modulation in strained p-type silicon thin films

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1. Abstract

This work aims to investigate the influence of mechanical pressure on the modulation of contact resistance between tungsten carbide probe tips (a metallike material) and thin silicon films. The characterization of the series resistance modulation was conducted using Pseudo-MOSFET devices. For this purpose, silicon-on-insulator (SOI) wafers were employed. This approach allowed for the extraction of electrical parameters with a reduced number of fabrication steps, aiming at the rapid prototyping of the devices.

2. Introduction

The engineering of electrical contacts in devices such as transistors is a highly relevant topic for the microelectronics industry, spanning from the earliest transistors to current technological nodes. The aggressive downscaling process currently employed progressively reduces the contact area, consequently increasing the series resistance of the devices, thereby diminishing their performance and raising costs associated with heat dissipation [1]. In this context, the industry has been exploring alternatives to decrease contact resistance by employing new materials and specific doping levels in source/drain regions.

The contact established between a metal and a semiconductor can behave as Schottky, acting as a rectifer or as ohmic, allowing current flow in both directions. These scenarios can be approached by the energy band model at the junction between the materials [2]. Alternatively, electrical measurements can also provide information about junction potentials, the type of contact established, and contact resistivity.

In this context, this work proposes to study the modulation of contact resistance in source/drain regions of MOSFET transistors. This was achieved by varying the mechanical pressure of probe tips on p-type silicon films. The proposal here was to establish a simple and effective method for reducing contact resistance in device prototypes without the need for numerous fabrication processes, which include lithography, ion implantation, metal deposition, and annealing. The experiments were conducted using a simple prototyping apparatus employing Pseudo-MOSFET (Ψ-MOSFET) devices [3] on silicon-on-insulator (SOI) wafers. The results demonstrate that contact resistance can be effectively modulated by reducing the Schottky barrier between the probe tips and the semiconductor. We consider this prototyping process to be interesting for the electrical characterization of semiconductors when no complex microfabrication facility is available.

3. Methodology

A. Silicon-on-insulator (SOI) wafers

Silicon-on-insulator (SOI) wafers consisting of a 340 nm thick Si-p doped film with approximately $5 \times 10^{15} cm^{-3}$ of boron on a 400 nm buried oxide (BOX) layer on a silicon substrate (bulk) were used.

B. Device fabrication

The center of the SOI pieces was protected with PVC tape to define the silicon mesa structure, thus preventing leakage current through the wafer edges and Si-SiO_2 interface. Subsequently, inductively coupled plasma (ICP) etching was performed in a hexafluoride sulfur (SF_6) and argon (Ar) environment. These steps resulted in Ψ-MOSFET device where the active region is the mesa structure with approximately 5 x 5 mm^2. The back region of the wafer serves as the back-gate, and the BOX layer acts as the gate dielectric.

C. Measurement and parameter extraction

For electrical characterization, measurements were performed using 2 tungsten carbide (WC) probe tips with a 4-point probe system, in conjunction with the Keithley 4200 - SCS electrometer. The probes have a diameter of 0.5 mm and are 1 mm apart from each other, featuring a conical tip with an end consisting of a circular section with a radius of 40 μm. The samples were placed on an aluminum metal electrode, which served as the gate electrode, while the two probe tips acted as source/drain electrodes. These probes are coupled to a spring system, allowing pressure adjustment on the substrate (up to 200 MPa).

4. Results and Discussion

Initially, we left the back-gate electrode floating and extracted the current-voltage curves between the source/drain probe tips (Fig. 1). It is clear that increasing the pressure results in an increase in current. Pressures of 100 MPa allow for an increase in current by more than an order of magnitude. This is due to the effect of reducing the Schottky barrier. However, the carrier density in the channel is still low to exhibit a linear curve.

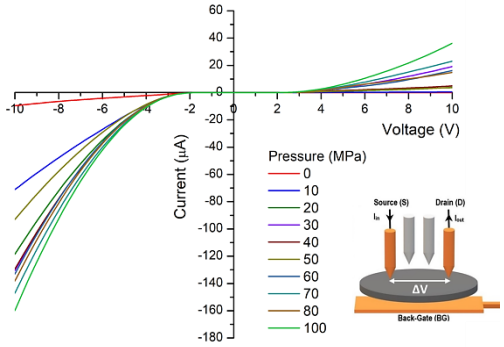

Fig. 1. *Current-voltage graph for different pressures applied to the sample up to 100 MPa.*

Additionally, a fixed voltage was applied to the back-gate (V_{GS} = 10 V) to invert the carrier density in the channel, which allowed obtaining the I_{DS} x V_{DS} curves in the triode region by parameterizing the pressure on the tips (Fig. 2). This curve illustrates that the contact becomes ohmic for the established inversion condition in the channel, and the contact resistance varies monotonically with the pressure on the probe tips.

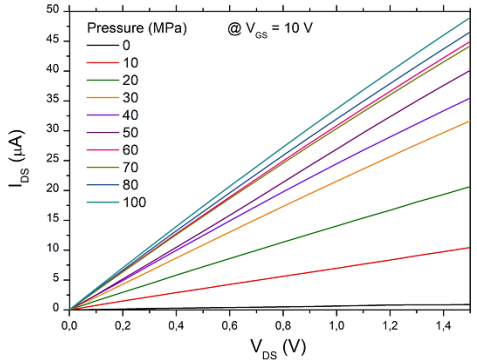

Fig. 2. *I_{DS} x V_{DS} graph with V_{GS} = 10 V for different pressures applied to the sample up to 100 MPa.*

Figure 3 shows the I_{DS} x V_{GS} and g_m x V_{GS} curves (for V_{DS} = 0.1 V), displaying the typical ambivalent behavior of Ψ-MOSFETs. The accumulation (V_{GS} < -2 V), depletion (-2 V < V_{GS} < 2 V), and inversion (V_{GS} > 2 V) regions are present. The threshold voltage (V_{TH} ~ 2.2 V) is clearly invariant with pressure, as its effect modulates the contact resistance and not parameters such as the interface charge density of Si-SiO_2.

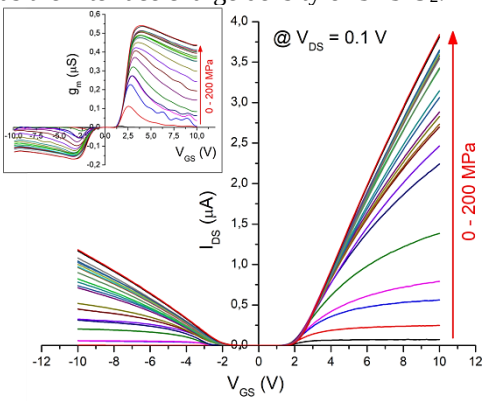

Fig. 3. *I_{DS} x V_{GS} graph for different pressures applied up to 200 MPa. The transconductance curve is presented in the inset for the same pressure range.*

It is interesting to note that transconductance increases monotonically with pressure as the series resistance of the device decreases, which should also reduce mobility degradation. Another relevant point is that the more significant variation of transconductance with pressure in the inversion regime than in the accumulation regime suggests that the series resistance decreased more for electrons than for holes.

The inset of Fig. 3 shows that, despite the transconductance increasing monotonically with pressure, it appears to saturate. In fact, Fig. 4 shows that the maximum transconductance stabilizes at its maximum value of 0.5 μS around 80 MPa. Pressures above this threshold do not result in a significant current gain.

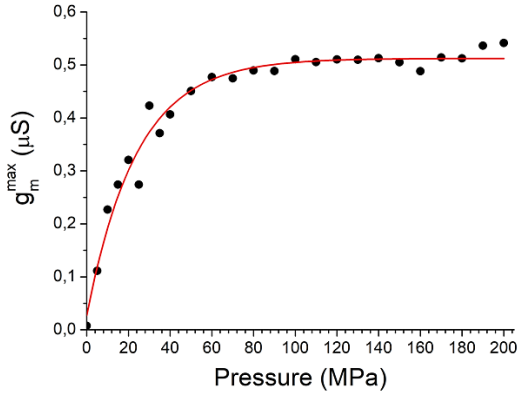

Fig. 4. *Graph of maximum transconductance (g_m^{max}) versus pressure for the fabricated Pseudo-MOSFET transistor.*

5. Conclusions

The results presented here show that the probe tips of 4-probes measurement system can be used for rapid prototyping of devices and extraction of characteristic curves, reducing manufacturing costs in cleanroom facilities. Pressures of approximately up to 80 MPa were sufficient to reduce the Schottky barrier and minimize the series resistance of Ψ-MOSFETs. Our research group is conducting advanced characterizations that may provide detailed insights into this phenomenon from a materials science perspective.

Acknowledgments

The authors thank CCSNano/UNICAMP for clean room facilities. This work was financially supported by CNPq (Grant No. 310021/2021-9 and 406193/2022-3 (NAMITEC)).

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Characterization of Switching Properties of ReRAM Devices by the Capacitance Measurements

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1. Abstract

This paper aims to present an analysis of the switching properties of Resistive Random-Access-Memory devices in relation to the capacitance variation of the Metal-Insulator-Metal structure. A capacitance spread was observed when a set of pulses at different amplitudes were applied to operate the devices in the Multi-Level-Cell regime. The devices demonstrate an increase in the capacitance from 2.0338 to 2.0344 pF/μm^2 from the pristine state to the maximum pulse width increment. This allows for the observation of multiple capacitive reactance states, demonstrating the quantization of the conductance, required for the application in in-memory computing systems.

Keywords- MIM; ReRAM; Resistance; Multi-level Cell; Capacitance.

2. Introduction

In the field of emerging memories, Resistive Random-Access-Memory (ReRAM) [1] constitutes an alternative for the development of high-density and ultra-low-power applications [2-3]. One of the most promising properties of the ReRAM devices is the capability of exhibiting multiple resistance states [4], enabling them to operate in a Multi-Level-Cell (MLC) regime [5], which is a property required for the development of in-memory computing systems [6-8]. Transition Metal Oxide (TMO) based resistive memories (OxRAMs) are considered one of the most viable solutions to implement artificial synapses for neuromorphic computing systems [9]. Typically, during a pulse set operation, the conductance of the device varies based on the pulse height, width, and number of pulses. In this work, an evaluation of the multiple switching properties [10] of ReRAM devices is performed by applying a set of pulses by varying the pulse width. The capacitance analysis of the Metal-Insulator-Metal (MIM) [11] structure correlates well with variations provided by a different set of pulses to the multiple conductance states of the devices.

3. Methodology and Devices Characteristics

The TMO-based devices were fabricated in 300 mm silicon wafers where an initial application of 10 nm of Ti followed by another of 50 nm of TiN, both via physical vapor deposition (PVD), constitute the bottom electrodes (BE). The insulating layer composed of HfO_2 was directly deposited above the TiN. The deposition was done using an atomic layer depositor (ALD) reactor where tetrakis (ethylmethylamido) hafnium was adopted as the Hf precursor, resulting in a 7 nm-thick layer of stoichiometric HfO_2. After the HfO_2 deposition, the top metal electrodes (TE) were fabricated with 5 nm ALD Ru followed by 5 nm of ALD TiN and 50 nm of PVD TiN, occupying a total area of 100 μm^2. The devices were fabricated at Tokyo Electron Limited (TEL) Labs.

The devices were characterized using the B1500A semiconductor device analyzer at the VLSI lab at the New Jersey Institute of Technology. To verify if the effect of the quantized switching [12] affects the MIM structure's capacitance values, different pulses [10] were applied to the top electrode of the devices, and the capacitances were measured immediately after each pulse application. For the amplitude variation, the pulses were applied from 1.5 up to 3.5 V in a 0.5 V step as shown in Fig. 1. The pulse width was kept at a fixed value of 1 ms. It is worth mentioning that a reset process [13] was applied at the end of each capacitance measurement.

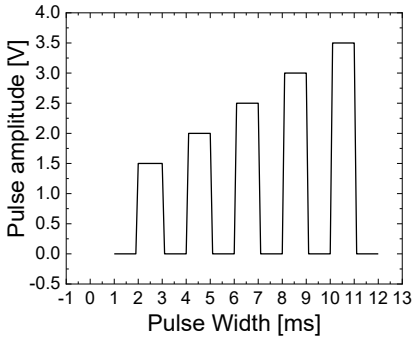

Fig.1. *Pulse scheme for the amplitude variation.*

4. Results

Initially, the capacitances were measured with the device in its pristine state, where the insulating layer has intrinsic defect concentrations. Subsequently, the capacitance was measured after applying pulses using different amplitudes and plotted as a function of the applied voltage on the top electrode. As shown in Fig. 2,

all the capacitance curves were measured at a frequency of 1 kHz. One can observe that all the capacitance curves show a parabolic dependence on the applied voltage. Concerning the capacitance's variation with respect to the voltage (-0.5V to +0.5V), the pristine capacitances vary from 2.0353, dropping to 2.0335 and increasing to 2.040 pF/μm^2. Also, it is important to note that the pulse application results in an increase in the overall capacitances. A larger spread of capacitance variation was observed at the lower capacitance levels. At higher voltages, the curves tend to converge to the same capacitance value.

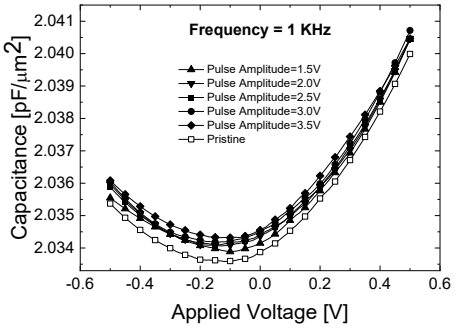

Fig.2. *Capacitances as a function of the top electrode voltage for different pulse amplitudes for 1 kHz frequency.*

To provide a better view of the capacitance increase with the amplitude variations, the capacitance for the applied voltages of -0.5, -0.12, and 0.5 V were extracted and plotted as a function of the pulse amplitude as shown in Fig. 3, where the capacitances in the pristine state are represented by closed symbols. The capacitance increases from 2.0353 to 2.0360 pF/μm^2, 2.0335 to 2.0343 pF/μm^2 and 2.0400 to 2.0404 pF/μm^2 from the pristine to the maximum pulse amplitude increment for the applied voltages of -0.5, -0.12, and 0.5 V. The fluctuations in the capacitance values can occur due to the time-constant dependence of defects in the dielectric and to the formation and migration of defects in the switching layer.

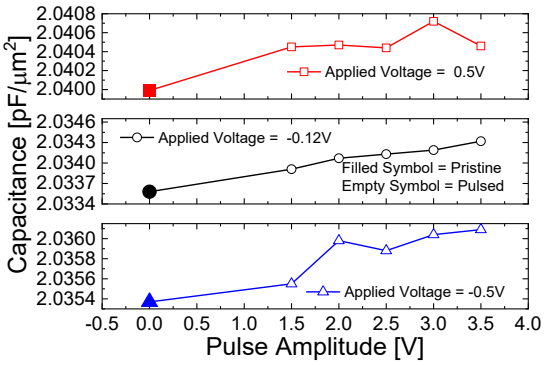

Fig.3. *Capacitances as a function of the pulse amplitude for 1 kHz frequency.*

The capacitive reactance (*Xc*) can be described as the resistance of a capacitor when an alternate current or signal is flowing through its terminals [14], and it was extracted using Eqn (1).

$$X_C = \frac{1}{2\pi f C} \qquad (1)$$

where *Xc* is the capacitive reactance (Ω), *f* is the frequency (Hz), and C is the capacitance (F).

In Fig. 4, *Xc* is presented as a function of the amplitude of the pulses. For the same pulse amplitudes indicated in Fig. 2, the amplitude variation promotes reductions of 781.968 to 781.692 kΩ, 782.544 to 782.282 kΩ, and 780.198 to 780.018 kΩ from the pristine state to the maximum amplitude value for the applied top electrode voltages of -0.5, 0, and 0.5 V, respectively. As the devices present multiple resistance states, the quantization of the conductance [12] can be observed, indicating the operation of the devices in the MLC regime.

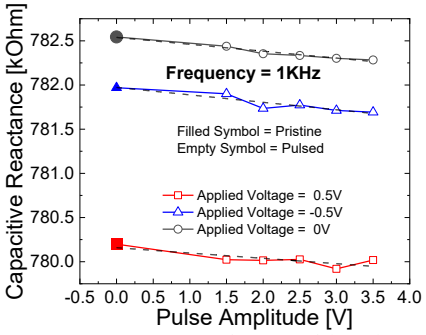

Fig.4. *The capacitive reactance as a function of the pulse amplitude for different TE voltages.*

4. Conclusions

This work has evaluated the switching properties of ReRAM devices through the capacitance measurements of the MIM structure. The analysis was carried out with different sets of pulse amplitudes to verify the influence of the capacitance in the multiple resistance states. It is shown that the capacitance increases with an increment in pulse amplitudes, which can be demonstrated by the capacitive reactance of the devices, exhibiting the quantization of the switching properties.

Acknowledgments

The authors thank the Brazilian funding agencies CAPES, CNPq, and FAPESP for the financial support and Drs. D.H. Triyoso, K. Tapily, R.D. Clark, S. Consiglio, S. Rogalskyj, K. Imakita, S. Lombardo, C.S. Wajda, and G.J. Leusink of TEL Technology Center, America.

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A comparative analysis of Bulk ISFET and ^{BE}SOI ISFET sensitivities

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1. Abstract

This work provides a comparative analysis of the sensitivities exhibited by conventional (bulk) Ion-Sensitive Field-Effect Transistor (ISFET) and Back Enhanced Silicon-On-Insulator (^{BE}SOI) ISFET. The study explores the devices behavior in different pH solutions to assess their sensitivity. The ^{BE}SOI ISFET shows better sensitivity than the conventional ISFET, and it also demonstrates variable sensitivity based on the programming gate voltage. These results highlight its potential for biosensing applications in future studies.

2. Introduction

The Ion-Sensitive Field-Effect Transistor (ISFET) plays a significant role in various applications, such as biomedical [1], environmental [2], contributing to advancements in diagnostics, environmental monitoring, and industrial process control. Its importance lies in the ability to detect ion variations, especially in aqueous solutions, enabling biosensors applications [3]. Furthermore, the ISFET is notable for its sensitivity to environmental changes and its capability to provide real-time responses. Its versatility and accuracy make it an essential component in research and technological developments related to ion detection and analysis in different contexts [4].

In this context, many research groups study how to fabricate different types of devices based on ISFET and increase the sensitivity for various applications. One of these groups, in Brazil, studied the fabrication and the electrical characterization of a bulk ISFET for Hydrogen Peroxide and pH sensing [5], in addition to proposing a new type of ISFET: the ^{BE}SOI ISFET [6].

3. Devices Characteristics

The devices were fabricated at Integrable System Laboratory (LSI), University of Sao Paulo. The conventional ISFET was made on p-type silicon wafer, with phosphorus diffusion to make a nMOS transistor. The result of the device and the schematic draw can be saw in Fig.1-A and Fig.1-B, respectively. The ^{BE}SOI ISFET was fabricated on a Silicon-on-Insulator (SOI) wafer and has no doping process to create any diffusion region. A platinum pseudo-electrode was used to bias the electrolyte on the gate region of the device in both of cases.

Unlike the conventional technologies, the ^{BE}SOI ISFET does not undergo an intentional doping process for the source and drain; it relies solely on the natural doping of the substrate. Consequently, the manner in which channel conduction is controlled differs from traditional and ^{BE}SOI ISFET. The ^{BE}SOI ISFET electrical behavior is based on ^{BE}SOI MOSFET [7]. The programming gate (Substrate contact) is responsible for defining the doping type in the channel region, inducing a form of doping due to the electric field, a phenomenon also referred to in the literature as electrostatic doping [8].

Due to this characteristic, it is possible for the device to conduct with both carriers, electrons and holes, by simply changing the polarization through the programming gate. In other words, if a positive enough voltage is applied to this contact, there will be an accumulation of electrons at the channel/buried oxide interface. Conversely, if a sufficiently negative voltage is applied, holes will be accumulated. In Fig.2 is possible to observe the n-type ^{BE}SOI ISFET results for pH sensing (2-A) and its schematic drawing (2-B).

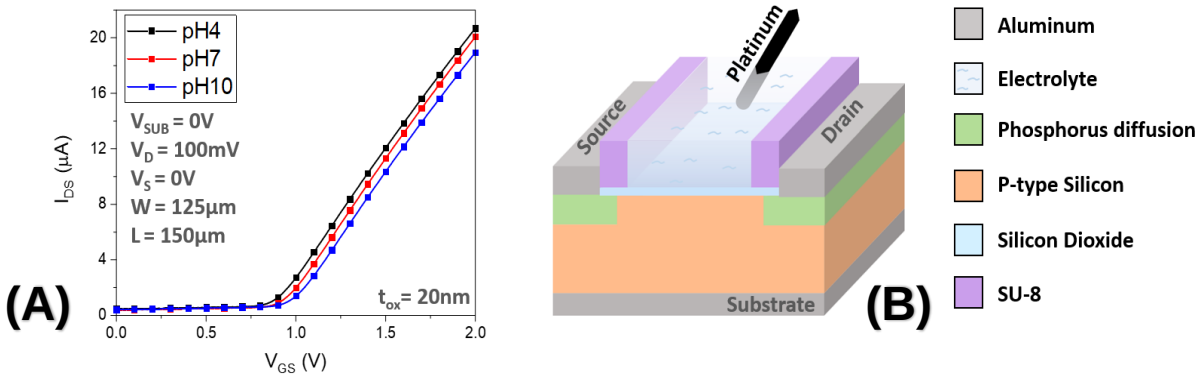

Fig.1. The Bulk ISFET pH sensing results (A) and the device schematic drawing (B).

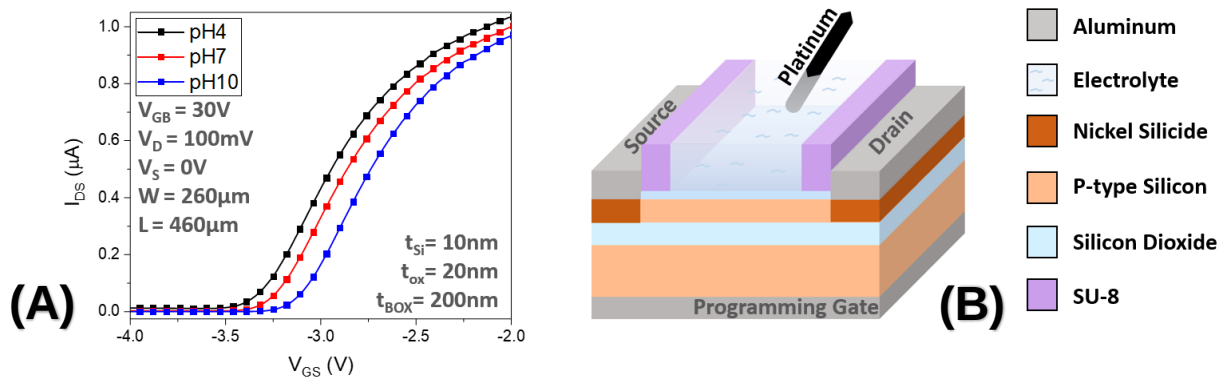

Fig.2. The [BE]SOI ISFET pH sensing results (A) and the device schematic drawing (B).

4. Comparison Analysis

To perform a comparative analysis between the conventional ISFET and the [BE]SOI ISFET, the sensitivity of the devices was defined as the variation in threshold voltage within the pH range of 4 to 10. The graph in Fig. 3. shows the sensitivity comparison between the devices.

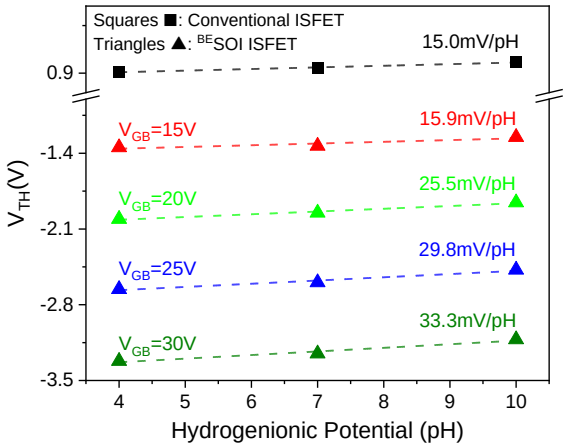

Fig.3. *Threshold Voltage as a function of Hydrogenionic Potential for conventional ISFET and [BE]SOI ISFET.*

In the comparison between conventional ISFET and [BE]SOI ISFET, a notable difference is observed in sensitivity. While the conventional ISFET maintains a constant sensitivity of 15 mV/pH, the [BE]SOI ISFET stands out for its variable sensitivity. Under different applied substrate voltage (V_{GB}) settings, the [BE]SOI ISFET exhibits higher sensitivities, suggesting a potential advantage in terms of flexibility and adaptation to diverse measurement conditions.

This variability in sensitivity makes the [BE]SOI ISFET more flexible and adaptable to different measurement conditions compared to the conventional ISFET, which has a fixed sensitivity.

5. Conclusions

A comparison analysis between the conventional ISFET and the [BE]SOI ISFET for pH sensing was conducted. Although the difference in sensitivity is not extremely pronounced at the lowest programming gate voltage settings (V_{GB}) for the [BE]SOI ISFET, when compared with the conventional ISFET, but it was possible to observe significant nuances in the adaptability and flexibility of the [BE]SOI ISFET to increase the sensitivity. This is due to its ability to vary sensitivity through different programming gate voltages, providing versatility that can be crucial in many measurement scenarios. Thus, this analysis demonstrates that the [BE]SOI ISFET has better sensitivity than the conventional ISFET and can be a promising device for biosensing applications.

Acknowledgments

The authors would like to thank FAPESP, CAPES and CNPq for the financial support.

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Development of a Microring Resonator to Detect Emerging Pollutants

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1. Abstract

This paper presents a simulation and fabrication of a microring resonator to detect residual contamination by azithromycin in water. In this optical device was used silicon dioxide (SiO_2, n=1.46) as inferior cladding and tantalum pentoxide (Ta_2O_5, n=2.05) as core.

2. Introduction

Pharmaceutical active compounds discard in water environment, with concentration varying from ng/L to µm/L, is one of the main safety and health concerns nowadays, which can cause adverse effects by the accumulation on the human body, when consumed without appropriate treatment [1,2].

This project is based on the fact that even small concentrations of some substance, like medicines, dissolved in water can alter its refractive index.

Optical microring resonator is very sensitive to detect any change on the device properties or environment, by changing the resonance frequency, which can be measured with accuracy in a bio-sensing device [3,4].

The device parameters were simulated and optimized by the technique Particle Swarm in Lumerical FDTD. The height of the pedestal is 1.0 µm, the thickness of the Ta_2O_5 core film is 0.25 µm, and the main parameters are described in Fig. 1.

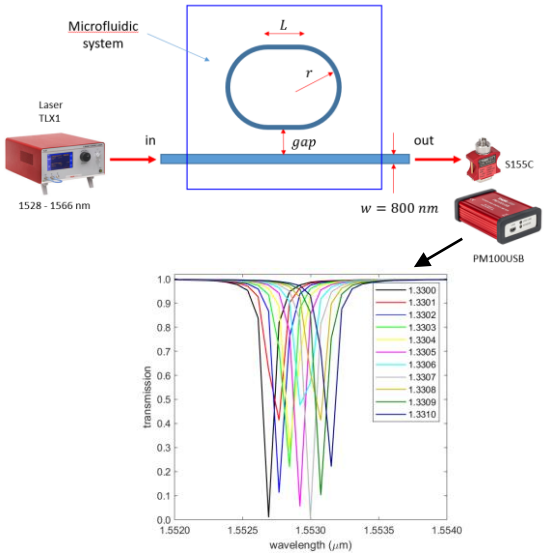

Fig.1. *Schematic of the device measurement and simulation of the frequency resonance.*

The dimensions of the microring resonator are described in Table I.

Table I. *Dimensions of the microring resonator*

r (µm)	L (µm)	gap (µm)
18.98	0.262	0.809
19.98	0.312	0.859
20.98	0.362	0.909
-	-	0.959
-	-	1.009

3. Methods and Results

The first step in the microring resonator fabrication by pedestal technique [5] is a dry oxidation to obtain a 150 nm SiO_2 film on a p-type silicon wafer (100).

In order to obtain a sub-micron structure, it is required a sub-micron photoresist [6]. A negative photoresist, ma-N-1405 (micro resist technology GmbH), presents a 500 nm thickness film at a spin-coating of 3000 rpm, and was used to define the waveguide and microring structures, on a direct-write photolithography system (MicroWriter ML3 Pro). The theorical critical dimension (CD) is calculated by [7]:

$$CD=k_1.\lambda/NA \quad (1)$$

Which gives a minimum pitch of 427 nm. In practice, individual lines with width of 800 nm were obtained, but the gap of 1.0 µm and below, did not separate. The double patterning technique was employed in order to resolve the pattern, described in Fig. 2. It involves two different masks that need to be aligned, one with the waveguide and the other with the microring, allowing the reduction of the minimum pitch by half [7].

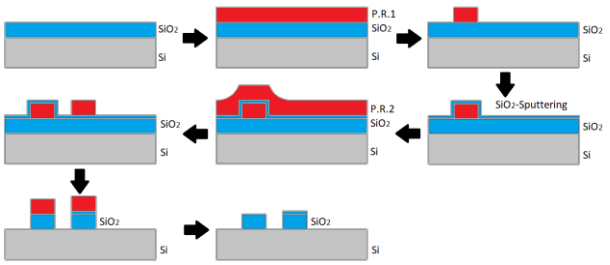

Fig.2. *Sequence of the Double Pattering process.*

A wet etching of the thermal SiO_2 is done in

Buffered Oxide Etching (6 NH_4OH (40%) + 1 HF (49%)), followed by the plasma etching of the silicon wafer, described in Table II.

Table II. *Plasma etching parameters*

Gas flow (sccm)			Pressure	Power	Time
SF_6	CHF_3	O_2	(mTorr)	(W)	(s)
26	10	15	75	100	120

1.8 µm of SiO_2 film is grown by wet thermal oxidation of the wafer, obtaining the pedestal structure.

The Ta_2O_5 core was deposited by DC reactive sputtering. In this process, the base pressure of the chamber reaches 7.5E-7 Torr, then oxygen is inserted to a partial pressure of 3.75E-4 Torr, and argon is inserted to a partial pressure of 1.35E-3 Torr, with a tantalum target (99.9%).

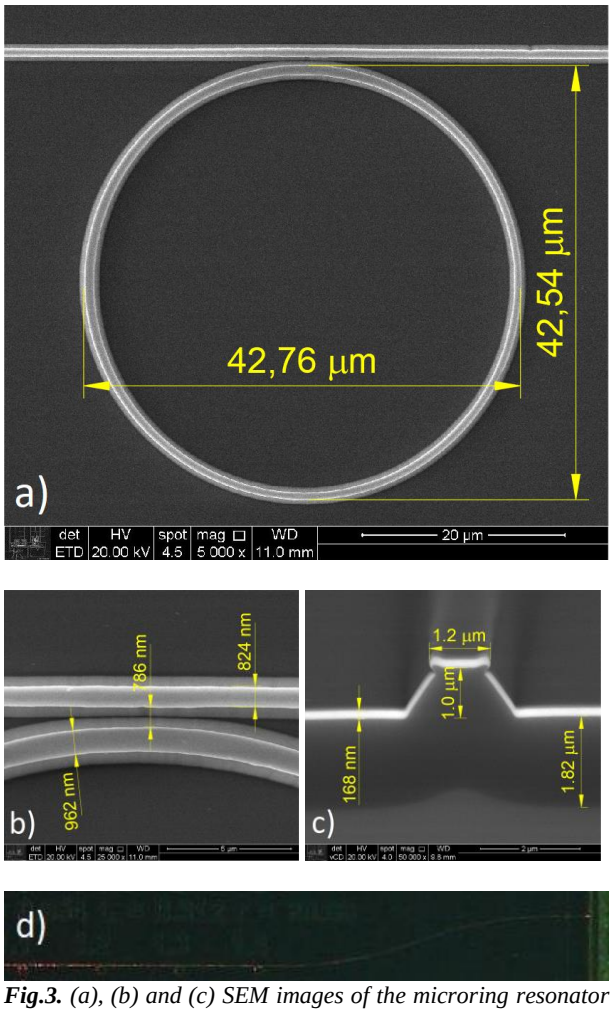

Fig.3. *(a), (b) and (c) SEM images of the microring resonator and (d) 633 nm laser propagation in the device.*

4. Conclusions

At the moment, it was possible to fabricate the microring resonator structure in respect to the dimensions determined by simulation, although the resonance frequency measurements were not yet successfully executed. A microfluidic system must be implemented in the near future for the analyses.

Acknowledgments

The authors acknowledge FAPESP and CNPq for the financial support.

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Post-Exposure Electrical Performance of Rectangular and ELT MOSFETs under Ionizing Radiation.

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1. Abstract

The current study aims to investigate the Total Ionizing Dose (TID) Effects on ELT MOSFET layouts and rectangular gate geometry MOSFET and compare their respective tolerance to TID. Specifically, it intends to determine whether the ELT Layout offers improved TID tolerance compared to a rectangular MOSFET for X-ray radiation. The behavior of the devices under the referred irradiation conditions suggests that, for the transconductance parameter, the ELT layout does not exhibit greater TID tolerance compared to a rectangular gate geometry device.

2. Introduction and Methodology

Power transistors are used in the most diverse systems and environments, including embedded circuits in the aerospace area, reactors, and particle accelerators, which require tolerance to ionizing radiation's effects [1]. In electronic devices, ionizing radiation can cause these devices to malfunction, altering their operating characteristics and may even result in the total loss of the device [2-3].

The Enclosed Layout Transistor (ELT) is a distinct MOS transistor layout characterized by a unique shape in which the channel region surrounds the drain or source regions. This structural feature eliminates the parasitic side transistor, which in rectangular transistors appears at the interface with the side insulation oxide, mitigating undesirable effects such as leakage current [2].

The effects of Total Ionizing Dose (TID) stem from the build-up of electric charge, primarily within the oxide layers and interfaces [1,4-5], induced by ionizing radiation exposure to devices. Given that the ELT structure incorporates a polysilicon area within the device and diminishes the oxide area, it emerges as a potential candidate for experiencing reduced damage from TID. Consequently, this study investigates the performance of the ELT MOSFET under applied doses of ionizing radiation totalling up to 300 krad(Si), administered at a dose rate of 100 krad(Si)/h.

The CTI (*Centro de Tecnologia da Informação*) designers group provides two integrated circuits (IC Power P-MOS Transistors, PPT), each one with five P-MOS devices in 0.6 µm SOI CMOS technology (fabricated by CEITEC – Brazil), three of them have the rectangular layout and the other two with ELT layout structures. The typical oxide thickness (t_{ox}) is 42 nm for those power devices, and all have the same dimensions of channel length and width.

The irradiation process used 10 keV X-rays at a dose rate of 100 krad(Si)/h [3]. Characterization occurred in a single step, with each circuit irradiated in two distinct bias states, accumulating a total dose of 300 krad(Si), followed by one week of Room Temperature Annealing (R.T.A). The initial bias state, ON MODE, involved setting the gate-drain voltage to -5V while maintaining the drain-source voltage at 0V. Conversely, the alternate bias state, known as the OFF MODE, entailed grounding all terminals.

The electrical I-V characterization utilized the NI-PXIe1062Q portable and modular system, with measurements conducted before, during, and after exposure to irradiation. Throughout the characterization process, the voltage across the Source-Drain terminals (V_{DS}) was maintained at -10 mV, applied in both irradiation modes, while the Gate-Source bias (V_{GS}) ranged from 1V to -5V. Measurements were taken at 20-minute intervals, with additional readings conducted one week later to assess recovery during R.T.A.

To ensure heightened precision, the extracted data underwent statistical analysis. The study's findings will include a comparative analysis of the average performance of the two ELT P-MOS and the average performance of three rectangular P-MOS devices for each irradiation mode.

In this way, specifically in this work, a systematic analysis of transconductance is presented, which is an essential characteristic for evaluating the performance and efficiency of power transistors through the rate of variation of the output current in relation to the change in voltage applied to the MOSFET gate.

3. Results

Transconductance (g_m) is a crucial electrical parameter, indicating the gate voltage's efficacy in controlling the drain current [6]. This parameter was extracted by taking the maximum value of the peak from the first derivative of an I_{DS} x V_{GS} curve.

Figure 1 shows the module of the variation of this parameter for one ELT Device due to the accumulation of radiation dose. A leftward shift is observable across all

devices and bias modes, suggesting the entrapment of charges within the oxide region [5].

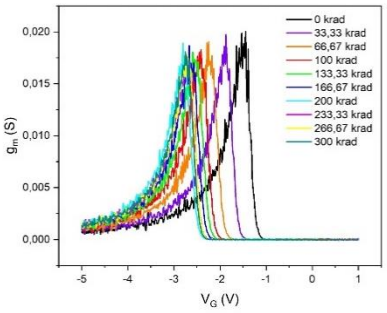

Figure 1 - g_m variation

Four graphs were plotted. The initial graph compares the conventional MOS's ON and OFF state modes, as depicted in Figure 2. Figure 3 illustrates a similar comparison performed for the ELT layout. Additionally, Figure 4 compares the rectangular MOSFET and the ELT in the OFF MODE. Finally, Figure 5 compares the two technologies in the ON MODE.

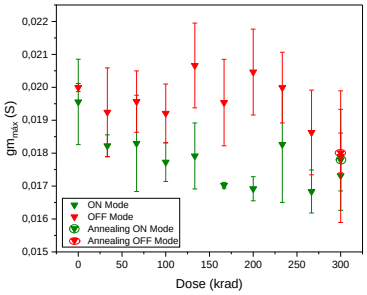

Figure 2 - Conventional Transistor Comparison (g_m)

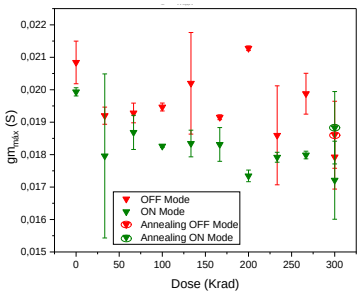

Figure 3 - Conventional Transistor Comparison (gm)

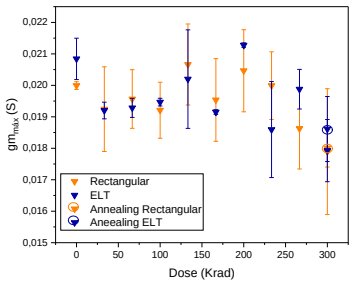

Figure 4 - Comparing Layouts in OFF MODE

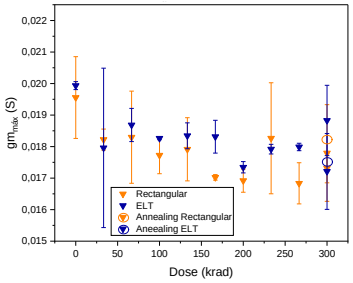

Figure 5 - Comparing Layouts in ON MODE

4. Conclusions

It is important to note that the devices are P-type, and the presented graphs exhibit their transconductance points in module. Therefore, a decrease in the maximum transconductance value indicates degradation in carrier mobility within the transistor [2]. It is evident that during the OFF mode of irradiation, the degradation of the parameter was lesser, which is expected since no channel is formed in this mode, resulting in fewer charge carriers in this region.

Moreover, it is noticeable that ELT transistors exhibit less variation in the parameter compared to rectangular ones, although some inflection points are observed where the transconductance value of the ELT transistor becomes higher than the rectangular transistor. This may indicate that regardless of the technology, X-ray radiation was sufficient to degrade both devices.

Regarding the transconductance parameter, the findings of this investigation indicate that the TID effects induced similar parametric degradation in the devices under test due to exposure to TID.

Acknowledgments

The authors acknowledge financial support from the funding agencies. FAPESP. Brazil 2022/09131-0, 2018/25225-9, 2020/04867-2, 2019/07764-1; CITAR: Proc. 01.12.0224.00; INCTFNA, Proc. 464898/2014-5; CNPq: 408800/2021-6, 301576/2022-0, 30360/2020-9.

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Analysis of the Low Voltage Cross-Coupled Oscillator

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Abstract

This work presents the analysis of a special case of the low-voltage cross-coupled oscillator, when the transistors act as ideal switches. A theoretical model to the oscillation frequency is presented and compared with that of an experimental circuit, showing good agreement.

1. Introduction

Cross-coupled oscillators are very useful circuits, with broad application on RF field [1]. The typical circuit includes a bias current at the sources of the transistors. The classical approach to the analysis is as a linear circuit [1]. However, like all other oscillators, the cross-coupled oscillator is a nonlinear circuit.

The inclusion of the bias current source demands the operation at higher voltages. In some applications, however, this level of voltage is not available, such as those powered by single photovoltaic cells.

A few authors analyzed the oscillator without a bias current source. Ge *et al.* [2] discuss the behavior or the circuit with a third order nonlinearity. Daliri & Maymandi-Nejad [3] present a model for a more generic circuit. They consider that the output voltages are equal, shifted each other by 180 degrees. Simulations should obtain an empiric value, which is related to the crossing point of the voltage waveforms at the drains. Machado *et al.* [4] model the oscillator with native transistors operating at ultra-low voltages using the small-signal approximation.

This work presents the analysis of a special case of the cross-coupled oscillator. The circuit does not have a bias current and operates with low voltage power supply. In the case studied, the transistors behave as ideal switches, being cutoff for a half period.

The rest of this work is organized as follows. Section 2 brings the working operation of the circuit and presents a proposal for the circuit model. Experimental results and their analysis appear on Section 3. Conclusions and future works are given in Section 4.

2. Working principle of the cross-coupled oscillator

The proposed oscillator is shown in Fig. 1. The circuit oscillates when a current step occurs at the cutoff of one transistor. Since an RLC circuit is formed by the inductance and parasitic elements of the gate of the other transistor, a decaying sinusoidal waveform is created at the drain. This waveform controls the oscillation of the circuit. Current and voltage waveforms are presented and discussed in Section 3.

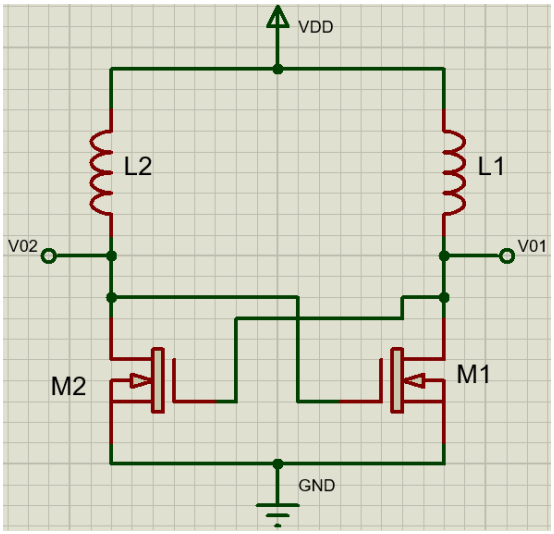

Fig.1. *Schematic diagram of the cross-coupled oscillator*

For the analysis of the circuit, one should consider the RLC circuit shown in Fig. 2. R1 and C1 are components from the gate of the transistor M1; R2 and C2 are components from the drain of the transistor M2, r is the series resistance of the inductor. It can be shown [5] that the current in this circuit is given by the formula:

$$i(t) = I_0 e^{-\sigma_0 t}\cos(\omega_D t + \theta_I) \qquad (1)$$

where:

$$\omega_D = \sqrt{\omega_0^2 - \sigma_0^2},\ \sigma_0 = \frac{R+r}{2L},\ \omega_0 = \frac{1}{\sqrt{LC}},$$
$$I_0 = \frac{I_M}{\cos\theta_I}, I_M = \frac{V_{DD}T_F}{2L},$$
$$\theta_I = \tan^{-1}\left[-\left(\frac{2}{\omega_D T_F} + \frac{R-r}{2\omega_D L}\right)\right].$$

V_{DD} is the power supply; T_F is the period of oscillation; R and C are respectively the equivalent resistance and capacitance seen by the inductance. L1 and L2 are identical: L1=L2=L.

According to Kirchhoff laws, the output voltage v_0 at the drain of any transistor is:

$$v_0(t) = V_{DD} - L\frac{di}{dt} - ri \qquad (2)$$

Applying (1) on (2) and after some algebraic

manipulation, one can prove that v_0 is given by the expression:

$$v_0 = V_{DD} + R_0 I_0 e^{-\sigma_0 t}[\sin(\omega_D t + \theta_I + \theta_D)] \quad (3)$$

where:

$$\theta_D = \tan^{-1}\left(\frac{R-r}{2\omega_D L}\right), R_0 = \sqrt{\frac{L}{C} - Rr}.$$

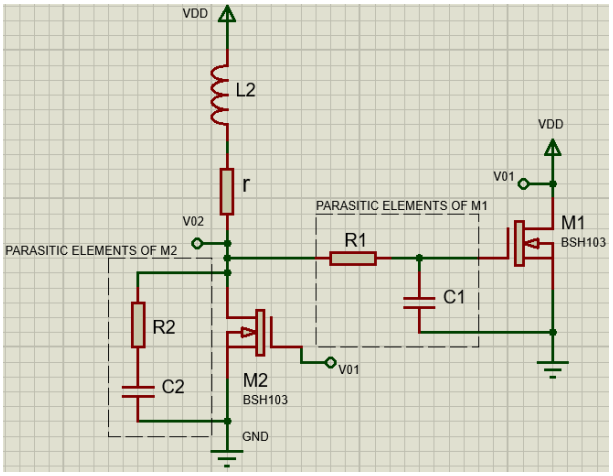

Fig.2. *Parasitic elements in the circuit*

3. Experimental results

The circuit was assembled using BSH103 transistors from NXP due to their high current capacity and low threshold voltage. Inductors are 3.3 µH with a series resistance of 0.3 Ω. Characterization of parasitic components using the method detailed in [5] found C=731 pF and R=18.0 Ω.

The circuit starts oscillating with 639 mV. In order to get clearer current and voltage waveforms, it was supplied with 2.0 V.

Current and voltage waveforms are shown in Fig. 3 (refer to Fig. 1). Voltage waveforms are quite close to sinusoids. Each transistor goes to cutoff during half period. Fig. 3 also shows the current waveform in L1. One can see a sinusoidal waveform in the cutoff period of M1, again confirming that the voltage waveform at the drain is sinusoidal. During the conduction of M1, the current is a ramp, because of the integration of a constant voltage at the inductor.

In order to obtain T_F, it is necessary to find the period where v_0 nulls, which corresponds to $T_F/2$. Eq. (3) does not have an analytical solution, so a numerical one should be provided. Applying the values from the characterization of the circuit, the oscillation frequency $f_F = 1/T_F$ found by the software MATLAB is 2.652 MHz. When compared to the experimental frequency (2.600 MHz), there is a deviation of 2.0 %.

This deviation can be explained by the nonlinear effect caused by the transition of the transistors through subthreshold region.

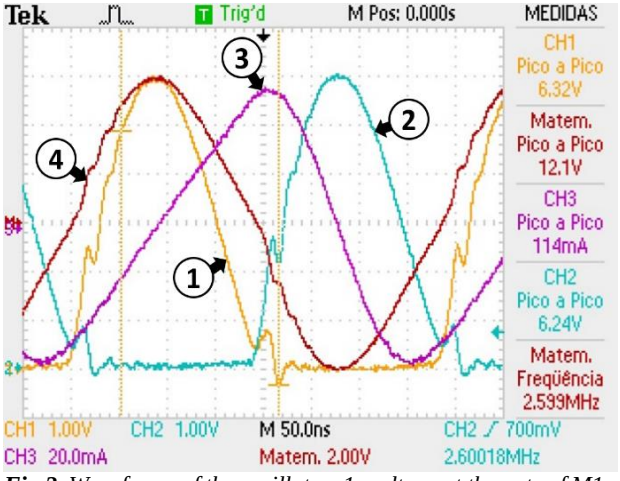

Fig.3. *Waveforms of the oscillator. 1- voltage at the gate of M1, 2- voltage at the drain of M1, 3- current at L1, 4- differential voltage between v_{01} and v_{02}.*

In this region, the modeling of the transistor as an ideal switch cannot be applied.

4. Conclusions and future works

A low-voltage cross-coupled oscillator was assembled and analyzed. An explanation to the working principle was presented. A preliminary model to the special case when transistors are considered as ideal switches was proposed. The theoretical result in the oscillation frequency is quite close to the experimental one.

A detailed analysis of the circuit, including the amplitude and shape of the voltage waveform is being prepared [5].

Acknowledgments

The authors would like to thank CNPq by the scholarship of R. G. Ono.

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Differential amplifier designed with Omega-Gate nanowire transistors.

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1. Abstract

In this paper, the Omega-gate nanowire transistor was modelled based on its experimental data, using the Look Up Table method and Verilog-A language, aiming to design a one stage differential amplifier with active load. The Cadence simulation was carried out for three different inversion conditions (gm/I_D): $7V^{-1}$, $8V^{-1}$ and $9V^{-1}$, where the best obtained values for voltage gain was 32dB and for Gain Bandwidth Product (GBW) was 118MHz.

2. Introduction

Through evolution and the advent of new technological nodes, current devices have followed Moore's Law on their scaling. Therefore, these devices present some problems as leakage current and short channel effects (SCE) [1]. Aiming to reduce or mitigate these undesirable effects new architectures were proposed like multiple gate devices that present better electrostatic coupling between the gate and the channel. One promising architecture is the Ω-gate nanowire [2].

The device that will be used in this work is the Ω-Gate nanowire fabricated in SOI wafer. This device emerged as a possible evolution for technologies such as planar bulk and fully depleted Silicon on insulator and SOI FinFETs. In addition, its manufacturing process is less complicated than the gate-all-around (GAA) [2], which has a similar technology. Due to its great electrostatic coupling between gate and channel, besides the higher immunity to SCEs, it also presents greater immunity to radiation, single event effects and in addition, it is suitable for high frequency and high voltage gain analog applications, as reported in [2] - [5]. In this work, the Ω -gate nanowires were modelled based on its experimental behavior and a single stage differential amplifier id designed to evaluate its potential for application in analog blocks.

3. Device and simulation characteristics

The measured device was fabricated at CEA-LETI, France, on a SOI wafer with buried oxide thickness of 145nm [3]. The studied device has the following characteristics: the gate material is composed of TiN covered by Poly-Silicon, the gate oxide (HfSiON) with an EOT of 1.3nm, the channel length of 100nm, the fin height (H_{NW}) of 10nm and fin width (W_{NW}) of 10nm. The effective channel width of the nanowire can be discovered by subtracting the portion of the channel not covered by the gate (5nm) from the circumference of the circle, which provides an effective width (W_{eff}) equal to 26.42 nm [3].

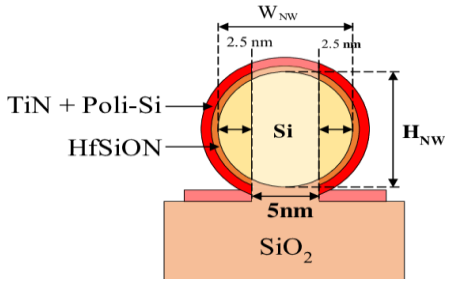

Fig.1. *Cross section of Ω-Gate nanowire [3].*

To develop an amplifier with an active load, Ω-Gate nanowire with a 100nm of channel length was measured. The transfer curves have a gate step of 10 mV and drain step of 50 mV, in order to obtain an accurate, Look Up Table and to model the device using a Verilog-A language. The model was created within the Cadence Virtuoso software. After that the differential amplifier is designed (figure 2) using a real Ω-gate nanowire behavior.

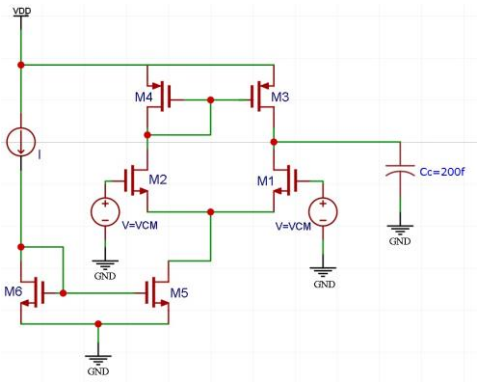

Fig.2. *Differential amplifier circuit implemented.*

4. Results

In order to validate the model, initially, P and N type transistors was simulated and their experimental behaviors were compared with the simulated ones as shown in Figure 3 and 4.

Figure 3 shows the drain current curves as a function of the gate voltage (V_G) for drain voltage (V_D) of 700 mV and Figure 4 shows the output characteristic (I_D x V_D) for V_G of 0.6V. From both figures, it is noticed that the obtained data from the modeled transistor fits very well with the experimental ones.

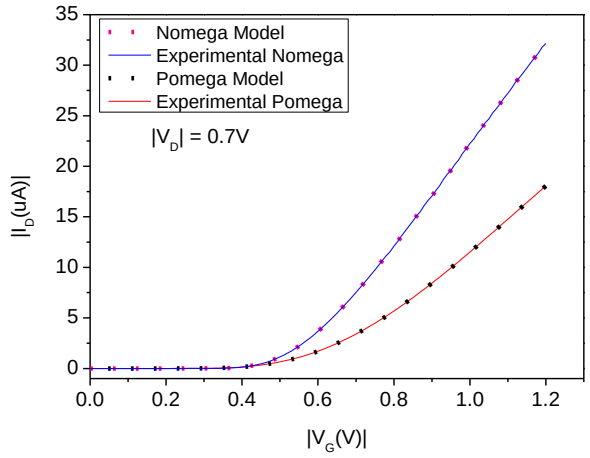

Fig.3.*Transfer curves (I_DxV_G) of modelled and experimental P and N type devices.*

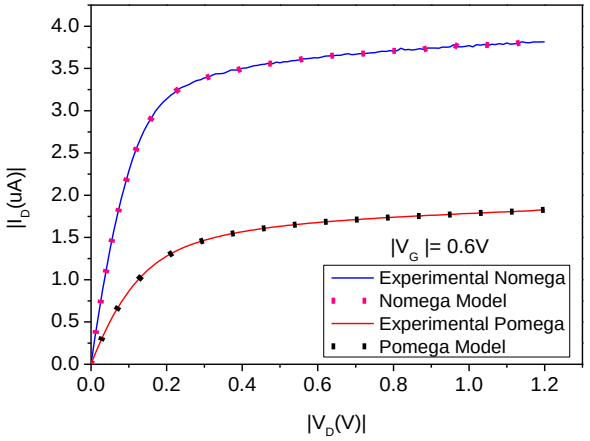

Fig.4. *Output curves (I_DxV_D) of modelled and experimental P and N type devices.*

The differential amplifier with active load illustrated by Figure 2, was simulated for three different inversion conditions (gm/I_D): 7V^{-1}, 8V^{-1} and 9V^{-1} .

Table 1 shows the main results of this work, such as voltage gain, GBW and power dissipation (Pd) across the circuit.

Table I. *Parameters referring to gm/I_D.*

gm/I_D (V^{-1})	7	8	9
Iss (µA)	44.544	34.643	28.186
Voltage gain (dB)	22.09	23.51	32.07
GBW (MHz)	118	109	99
Pd (µw)	160.3	123.7	101.5

Figure 5 shows the voltage gain as a function of frequency. The highest gain (32.4dB) was obtained for higher gm/I_D (9V^{-1}) and the lowest gain (22.09dB) for the gm/ I_D of 7V^{-1} following the same intrinsic voltage gain of the transistors. The opposite trend is observed for GBW since its parameter is proportional to the transconductance value.

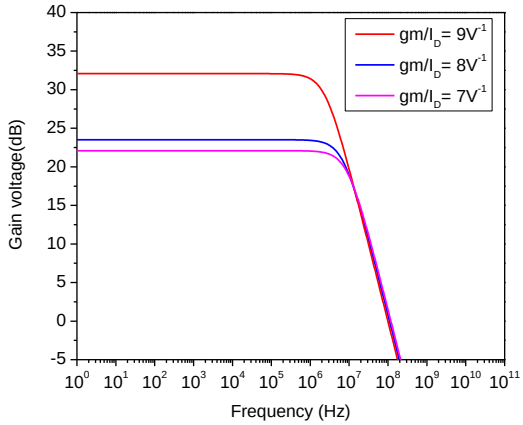

Fig.5.*Gain as a function of frequency.*

5. Conclusions

The paper presents an actively charged differential amplifier that was designed using modeling of a real nanowire omega-gate transistor. The simulation referring to the differential amplifier was carried out for three different polarizations (7V^{-1}, 8V^{-1} and 9V^{-1}), where the highest gain was obtained for higher gm/I_D (9V^{-1}) and the lowest gain for lower gm/I_D (7V^{-1}). Therefore, if we want to obtain greater gain but less GBW, we must use polarization 9V^{-1}, otherwise we must use the lowest polarization 7V^{-1} .

The next step of this work is to use the same polarizations and this first stage to develop a Low-drop out voltage circuit.

Acknowledgments

The Authors thank UNIVESP for the financial support, CEA-LETI for providing the devices used in the measurements and the LSI USP Group for providing the software and equipment for measurements.

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MISHEMT multiple channels influence on intrinsic voltage gain

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1. Abstract

This study delves into the MISHEMT device, focusing on how multiple conductions affect its intrinsic voltage gain (Av). We find that the total I_{DS} comprises components linked to different current channels, a MOS channel and a 2DEG channel. The device's output characteristics exhibit dual V_{DS} saturation, resulting in a double plateau in the saturation region. This behaviour is influenced by V_{GS}, making output characteristics and analog parameter extraction dependent on both V_{GS} and V_{DS}. The intrinsic voltage gain rises from 37 dB to 40 dB due to the V_{EA} increment from 283 V to 490 V in the second plateau, where 2DEG conduction dominates.

2. Introduction

Wide bandgap semiconductors have gained widespread acceptance in RF electronics for their capacity to operate efficiently at high frequencies [1], showcasing notable power gains at 10 GHz [2]. Among these, the GaN Metal-Insulator-Semiconductor High Electron Mobility Transistor (MISHEMT) emerges as a promising candidate for power applications, offering high current levels, elevated breakdown voltages, and a reduced gate current leakage when compared with its predecessor, the HEMT [3, 4], that has a Schottky contact as its gate structure.

Due to internal polarizations and bandgap mismatch present in III-Nitrides heterostructures, a conduction band discontinuity is generated at the MISHEMT's heterointerface, that creates a very thin region where the conduction band is lower than the Fermi level, as shown in Fig. 1. In this region, electrons do not need any additional energy to become free. This creates a current channel called 2-Dimensional Electron Gas (2DEG) [5], which plays as primary current channel in most heterostructure-based devices.

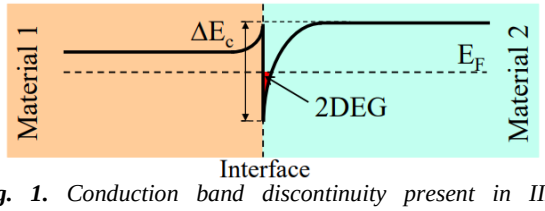

Fig. 1. *Conduction band discontinuity present in III-N heterostructures.*

Modern devices incorporate a few nanometers thin spacer layer between the main heterojunction to boost the concentration of carriers within the 2DEG [6], and promote the formation of two distinct 2DEGs. Since they are so close together, their activation voltages, are so close that they are effectively treated as one unique activation voltage [7, 8].

While having the 2DEG as its main channel, the MISHEMT's gate insulator introduces an additional electron channel that accumulates at the gate insulator/semiconductor interface, which is called MOS channel due to its intrinsic dependence on the gate insulator and structure. The MOS channel only significantly contributes to drain current (I_{DS}) when the gate to drain and gate to source electrodes distances (L_{GD} and L_{GS}) are short, facing a lower resistance. Each channel has its own activation voltage, determined by factors such as the distance between the gate electrode and the channel and its inherent characteristics [7, 8].

How the MOS channel influence on I_{DS} and how it shapes the device's DC behaviour is studied in this work. This study proposes an analysis of output conductance (g_D), Early voltage (V_{EA}) and Intrinsic Voltage Gain (Av) in order to validate the MISHEMT multiple channel characteristics potential for analog applications.

3. Device characteristics

The cross-sectional view of the MISHEMT is depicted in Fig. 2. Its gate structure consists of 2 nm Si_3N_4 as gate insulator, 15 nm AlGaN barrier layer, 1 nm AlN spacer layer, and 300 µm GaN buffer layer.

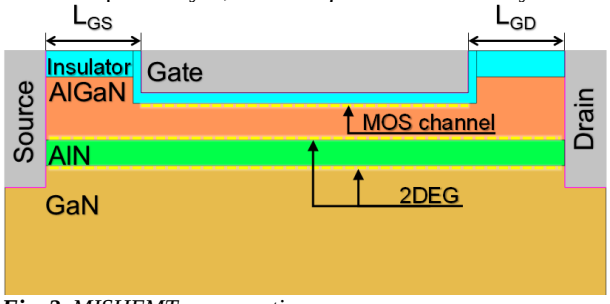

Fig. 2. *MISHEMT cross section.*

4. Results and analysis

Fig. 3 presents the MISHEMT electron concentration, where it can be observed high carrier densities at the three mentioned regions: the 1st interface (Si_3N_4/AlGaN) related to MOS channel, the 2nd interface (AlGaN/AlN) and the 3rd interface (AlN/GaN) related to 2DEG channels.

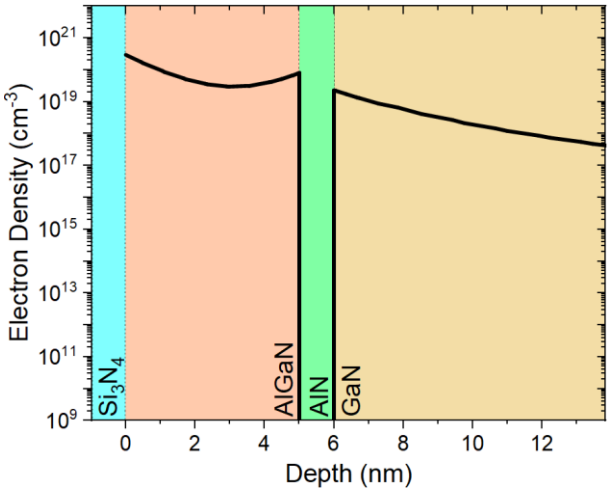

Fig. 3. *MISHEMT electron concentration.*

Fig. 4 presents the MISHEMT drain current (I_{DS}) as a function of the drain voltage (V_{DS}) for different gate voltages (V_{GS}).

For a V_{GS} from 0.0 V down to -2.0 V it is possible to see that double plateau is present. This characteristic points to a double channel saturation, each one having a different V_{DSsat}. For more negative V_{GS} the two plateaus start to merge with each other, until V_{GS} reaches -3.2 V where only one plateau can be seen.

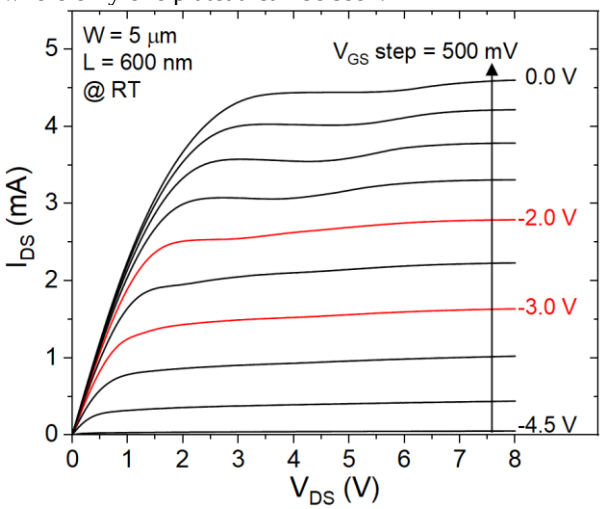

Fig. 4. *Drain output currents for various gate biases.*

The internal polarization is responsible for the natural formation of the 2DEG channels, without the need of external voltage application, and do not contribute to the electron accumulation at the Si_3N_4/AlGaN interface. The gate electrode and V_{GS} are responsible for the electron accumulation at the Si_3N_4/AlGaN interface and for the depletion off all the channels. This means that the depletion region has to compete with the internal polarization in order to shut the 2DEG channel off. Also, since the depletion region created by negative V_{GS} is generated at the upper part of the semiconductor and is augmented towards deeper parts of it for more negative V_{GS}, the more distant the channel is from the gate electrode, the more negative V_{GS} is needed to shut deeper channels off.

With this it can be concluded that the I_{DS} x V_{DS} only plateau for more negative V_{GS} is related to 2DEG channel saturation. For more positive V_{GS} it can be noted that g_D for higher V_{DS} (2nd plateau) behaves the same as for the 2DEG channel saturation for more negative V_{GS}. This indicates that the 1st plateau for more positive V_{GS} is related to the MOS channel, while the 2nd plateau is related to the 2DEG channel.

Since MISHEMT behaviour depends on MOS and 2DEG conductions, in order to extract g_D, the V_{EA} and Av, two different points of the experimental I_{DS} x V_{DS} were chosen for each applied V_{GS}. The results are shown in Table I and Fig. 5.

Table I shows the extracted analog parameters from experimental data at room temperature.

Table I. Experimental analog parameters for 2 values of overdrive voltage extracted in the first and second plateaus.

V_{GS} (V)	Output curve region	gm_{sat} (mS/µm)	g_{Dsat} (µS/µm)
-0.8	1st plateau	0.185	4.60
	2nd plateau	0.164	3.33
1.3	1st plateau	0.195	4.62
	2nd plateau	0.187	3.75

Fig. 5 shows the intrinsic voltage gain (Av) for different biasing conditions at room temperature related to both plateaus. These biasing conditions are slightly different from the results shown in Table 1.

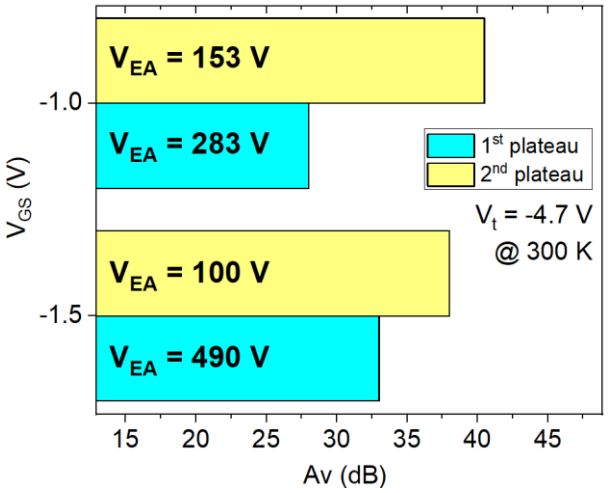

Fig. 5. *Intrinsic voltage gain and Early voltage for different bias conditions at 300 K, related to both plateaus.*

4. Conclusions

The influence of MISHEMT multiple channels on the device's Av is analyzed. The multiple channels exhibit different activation and saturation voltages, that are responsible for different V_{EA}, g_D and consequently Av at a fixed V_{GS}.

The double conduction is responsible for a new increase on I_{DS} that causes a double saturation effect to appear on the output curves. Because of this, the DC analog parameters change for both V_{GS} and V_{DS}. It also is responsible for a high electron concentration in the entire barrier layer.

When increasing V_{GS} it is unexpected that Av rises, because it is proportional to gm and V_{EA} and inversely proportional to I_{DS} and g_D. The high carrier concentration maintains an I_{DS} increase with V_{GS} increase, but the 2DEG channels saturations offer a great increase in V_{EA}, which is linked to a low degradation of g_D. V_{EA} increases from 100 V on the 1st plateau to 153 V on the 2nd plateau, leading to an increase in Av from 37 dB to 40 dB. For these reasons the MISHEMT appears as an interesting option for analog applications.

Acknowledgments

The authors acknowledge grant 2023/14492-4 Sao Paulo Research Foundation (FAPESP), CNPq and CAPES for the financial support.

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Low-Temperature Calibration of TCAD Simulations for Stacked Nanowire

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1. Abstract

This study presents a calibration method for simulating 2-level stacked nanowire devices in the temperature range from 300K to 150K. The method focuses on ensuring accurate modeling of device behavior under varying temperature conditions. Validation using experimental data at 300K and 150K demonstrates good agreement, confirming the effectiveness of the proposed approach.

2. Introduction

To reach the requirements of Moore's Law, MOS transistors were miniaturized and eventually achieved their physical size limit in planar technology. Multiple gate transistors, such as Nanowires (NW), have been demonstrated as a good alternative to continue the reduction of this device's dimensions, thanks to their better electrostatic gate control [1], which minimizes short-channel effects (SCE). The Stacked Nanowires hold significant potential for upcoming technological nodes by enhancing current density in the same area consumed by the device [2].

In TCAD simulations, physical models dictate the macroscopic behavior of FET, such as the carrier mobility. However, without proper configuration, TCAD simulators may fail to describe devices at the nanometer scale [3], particularly at low temperatures [4]. It is important to calibrate the simulator model parameters based on experimental data, as reliable TCAD simulation is a crucial tool for understanding the physical behavior of this promising device in design technology co-optimization (DTCO).

This study aims to show a calibration method for simulating a stacked nanowire over a temperature range from 300K down to 150K, utilizing experimental data.

3. Methodology

The simulations were performed using the Sentaurus Workbench (SWB) software. The structure was made using the Structure Editor (SDE) and is composed of 2-level n-type stacked SOI NWs, with a channel length (L) of 100nm, a fin width (W_{FIN}) of 10nm, and a fin height (H_{FIN}) of 10nm. The gate stack is formed by a thin layer of SiO2 followed by an HfSiON as the high-k material, with an effective oxide thickness (EOT) of about 1.3nm, TiN as the metal gate, and a polysilicon layer for the contact. Fig. 1 presents the device's perspective and cross-section view, indicating its main dimensions and contacts.

Curves of drain current (I_D) *versus* gate voltage (V_G) from 0V to 1.2V, with a drain bias of 25mV, were simulated using the Sdevice tool with the following models: Fermi Statistics; Altermatt model for Ionization; Auger and Shockley Read Hall (SHR) with doping and temperature dependencemodels for recombination; OldSlotBoom model for the bandgap narrowing; Philips Unified Mobility Model (Phumob) and Lombardi for the mobility calculate and their degradation with the electric field.

Experimental data of stacked nanowires fabricated at CEA Leti [2] with the same geometry characteristics were used to calibrate the simulation.

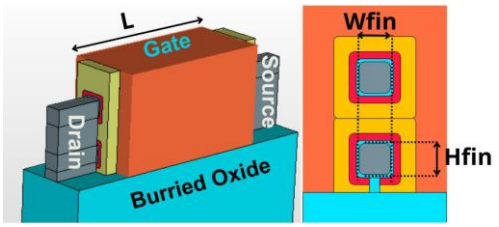

Fig.1. *Perspective and cross-section view of a stacked nanowire with 2-level.*

4. Discussion and Results

Initially, the simulator parameters were defined based on existing works [4-6], with adjustments made to parameters from the Phumob, Lombardi, and Altermatt models to align with low-temperature simulations.

Room temperature calibration was performed by adjusting the parameters from equations (1) and (2) from Phumob and Lombardi models, respectively.

Eq. (1) describes the mobility contribution due to lattice scattering, where T is the absolute temperature, μ_{MAX} is maximum carrier mobility and θ is a fitting parameter controlling the temperature variation on the mobility.

$$\mu_L = \mu_{MAX} (T/300)^{-\theta}. \quad (1)$$

Eq. (2) describes the mobility degradation due to surface roughness, where E⊥ is the perpendicular electric field, E_{REF} is a reference value of the electric field, and A*, δ, η are fitting parameters.

$$\mu_{SR} = (((E_\perp/E_{REF})^{A^*}/\delta) + (E_\perp^3/\eta))^{-1} \quad (2)$$

The parameter μ_{MAX} from (1) influences the linear region of the I_D-V_G curves and the peak of the transconductance (gm) *versus* V_G. The parameter δ from

(2) influences the mobility degradation in high V_G regions, with minimal effect on the linear region. Fig. 2 illustrates the I_D-V_G final calibration simulation at 300K compared to the experimental data showing a good agreement to it, complementary, Fig. 3 shows the transconductance curve.

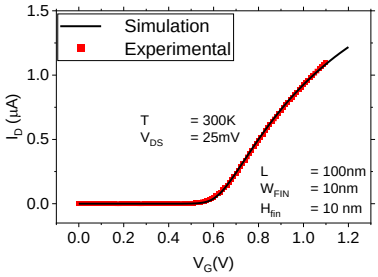

Fig.2. *Comparison of I_D x V_G curves between experimental and simulation data at 300K.*

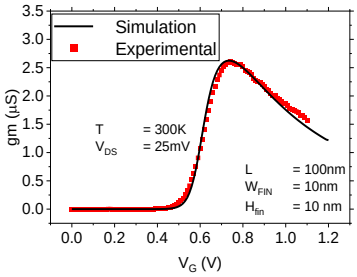

Fig.3. *Comparison of gm x V_G curves between experimental and simulation data at 300K.*

The temperature-dependent calibration is required to adjust the θ parameter in equation (1). This parameter governs the temperature dependence of the transconductance peak and was fine-tuned to achieve good agreement with experimental data. Fig. 4 and 5 depict the I_D-V_G curves at 200K and 150K, respectively, while Fig. 6 and 7 illustrate the transconductance.

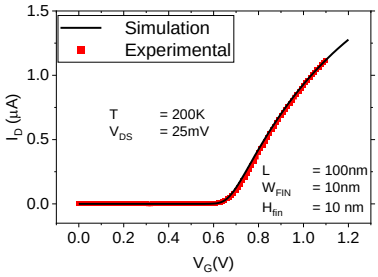

Fig.4. *Comparison of I_D x V_G curves between experimental and simulation data at 200K.*

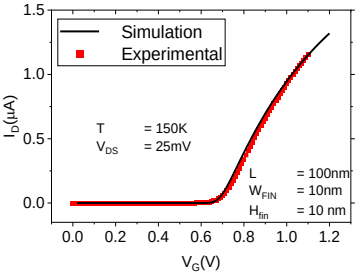

Fig.5. *Comparison of I_D x V_G curves between experimental and simulation data at 150K.*

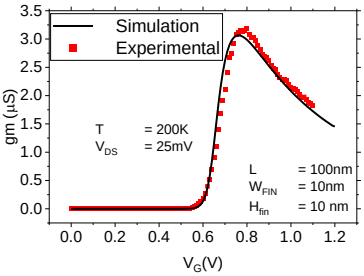

Fig.5. *Comparison of gm x V_G curves between experimental and simulation data at 200K*

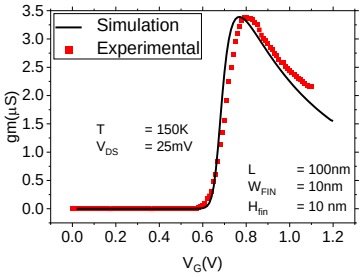

Fig.6. *Comparison of gm x V_G curves between experimental and simulation data at 150K*

5. Conclusions

In summary, our study demonstrates the efficacy of temperature-dependent calibration for aligning simulated and experimental data in two-level stacked nanowire devices.

Acknowledgments

The authors thank CAPES and FAPESP (2023/08530-0) for funding this project. We also thank to Jaime Calçade for providing the experimental data used in this study.

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Design and Implementation of Layouts for a 4-Bit Counter for the 180 nm Technology Node

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Abstract – In this paper, a 4-bit counter based on CMOS technology with a 180 nm node was developed. This device aims to integrate a partial shading identification system into photovoltaic panels and optimize the energy efficiency of these systems. Therefore, an operating frequency fixed at 32 MHz resulted in a manufacturing layout of 1395 µm², demonstrating efficient compactness.

1. Introduction

The partial shading in photovoltaic panels occurs when some modules are in shadowed areas while others are exposed to direct sunlight. This disparity generates overheating and heat dissipation regions, compromising solar panels' lifespan and efficiency [1]. Faced with this issue, the design of a partial shading identification system has been proposed, comprising the implementation of components such as logic gates, oscillators, multiplexers, and counters.

Each signal originating from the solar panel modules is connected to the inputs of the multiplexer, whose selector bits are defined by the outputs of a counter synchronized by the oscillator. This arrangement enables a systematic and continuous scan of the photovoltaic panel, aiming to detect adverse behaviors that could compromise the system.

The scope of this study is to develop a 4-bit counter with high operating frequency and low power consumption, suitable for 180 nm technology.

2. Materials and Methods

A. Implementation of the counter

To simplify the circuit, the use of D flip-flops was chosen, based on the principle of the master-slave system [2]. Consequently, a D flip-flop sensitive to the rising edge is obtained.

Additionally, pause and reset functions were added to the counter, identified as Enable (E) and Reset (R), respectively. To ensure robustness and proper operation, the counter must operate synchronously. Therefore, a multiplexer was implemented following the logic in Table I, connected to the D input of the flip-flop [3].

Table I. *Truth table of the multiplexer (X = don't care).*

E	R	D	Y
0	X	X	Q
1	0	X	D
1	1	X	0

Note that Y is the output of the multiplexer, Q is the counter output, and D is the current given value. The counter has a truth table, described as,

$$Qn = Z \Rightarrow Qn + 1 = Z + 1, \quad (1)$$

where counting starts from Z = 0 and progresses to the maximum count value of Z = 15, following a cyclic sequence [4]. Based on this, it is possible to perform minimization using the Karnaugh Map, resulting in expressions corresponding to the combinational circuits,

$$D3 = Q3 \oplus Q2Q1Q0 \quad (2)$$
$$D2 = Q2 \oplus Q1Q0 \quad (3)$$
$$D1 = Q1 \oplus Q0 \quad (4)$$
$$D0 = Q0' \quad (5)$$

where Dn is the D input of flip-flop n and Qn is the output of flip-flop n [5].

B. Circuit Sizing

A Generic Process Design Kit (GPDK) of 180 nm was used, where NMOS and PMOS transistors have the same transconductance. Additionally, this GPDK defines a minimum width (W) of 400 nm. Therefore, Wn = Wp = 400 nm was used for the inverters, which served as the basis for impedance matching for the rest of the circuit.

3. Results and Discussions

The circuit diagram for the D flip-flop has been implemented, as shown in Fig. 1.

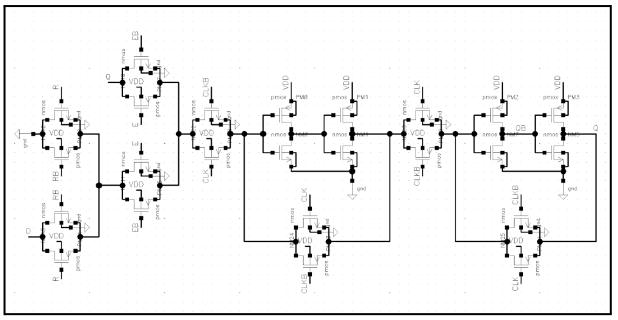

Fig.1. *Flip-flop D from software Virtuoso Cadence®.*

Fig. 2 shows the implementation of the 4-bit counter diagram. In a complementary way, Fig. 3 shows their respective characteristic curves with a simulation for an

operating frequency of 32 MHz.

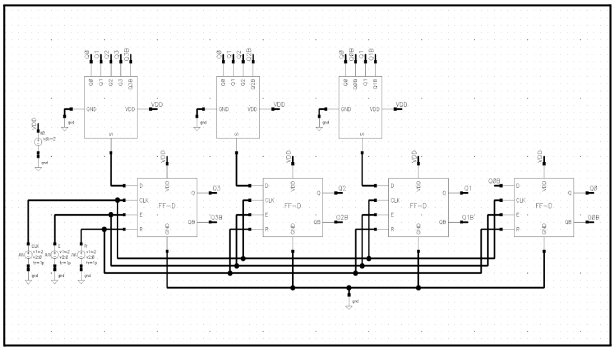

Fig.2. *4-bit counter from software Virtuoso Cadence®.*

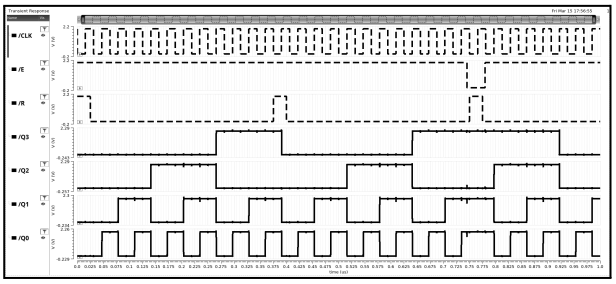

Fig.3. *Characteristic curves of the 4-bit counter from software Virtuoso Cadence®.*

From the validation of the 4-bit counter through simulation, the fabrication layout seen below in Fig. 4 was created. This circuit has dimensions of (43.2 x 32.3) µm and an area of 1395 µm².

In the next step, we intend to integrate the counter with other logic circuits (oscillator and multiplexer), migrating from the 180 nm GPDK to the 65 nm technology from Taiwan Semiconductor Manufacturing Company (TSMC).

4. Conclusions

The 4-bit counter demonstrates counting capacity from 0 to 15, in addition to presenting an adequate response to Enable and Reset control signals, operating at a frequency of 32 MHz. Expansion of counting capacity can be carried out through circuit cascading, enabling the construction of counters with a greater number of bits.

Acknowledgments

This project was funded by the Eldorado Research Institute (Finance code - ELD-SSJ14676), which also monitored the development of this project from 09/18/23 to 02/29/24. The Authors would like to thank Nelson Vitor Augusto from UNICAMP for invaluable technical support.

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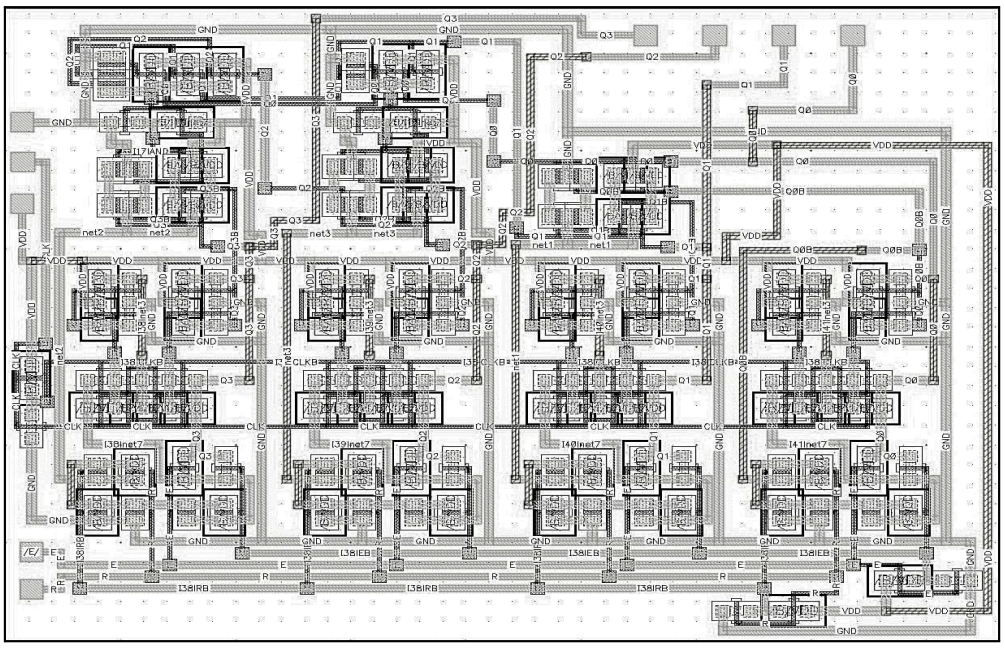

Fig.4. *Fabrication layout of the 4-bit counter from software Virtuoso Cadence®.*

Performance Analysis of an Optical System with Mach-Zehnder Interferometer and Semiconductor Optical Amplifier

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1. Abstract

This paper presents the study of the performance of an optical system composed of a Mach-Zehnder interferometer, semiconductor optical amplifier and Bragg grating fiber. The system was simulated in OptiSystem software from OptiWave Corporation and analyzed in terms of bit error rate (BER) and Q factor for different bit sequences and input powers.

2. Introdution

Optical telecommunications systems play a key role in transmitting data at high speeds and over long distances. The Semiconductor Optical Amplifier (SOA) is an essential component in these systems, providing signal amplification and data processing. However, SOA is subject to non-linear effects such as cross-phase blending (XPM) and cross-gain modulation (XGM), which can compromise system performance [1]. In addition, the presence of a Bragg Grating in SOA can significantly influence its behavior, affecting the generation and amplification of optical signals [2].

Recent research has explored combining semiconductor optical amplifiers (SOA) with optical interferometers to create all-optical logic gates [3,4]. In [3], for example, the use of a Michelson interferometer with SOA and Fiber Bragg Grating (FBG) to implement an optical NOR logic gate at 10 Gb/s is investigated, aiming at high-speed processing and analysis of non-linear effects. In turn, in [4] fully optical "AND" logic gate schemes with three inputs are simulated and experimentally studied, in which the proposed gate exploits the non-linearities of the semiconductor optical amplifier Mach-Zehnder interferometer (SOA-MZI).

In this work, we present and analyze the performance of an optical communication system that implements the Mach-Zehnder interferometer (MZI) and a semiconductor optical amplifier (SOA) and Fiber Bragg Grating (FBG).

3. Materials and Methods

The system proposed in this work was simulated using the OptiSystem software and the Q-Factor and Bit Error Rate (BER) for the simulated system were analyzed.

A. Design of optical communication system with Mach-Zehnder interferometer

The optical communication system analyzed in this study is presented in Figure 1. The transmitter operates with two input signals, A and B, generated by the Bit Sequence Generator, with the Optical Gaussian Pulse Generator at frequencies of 1550 and 1550.1 nm, respectively, with input powers of 0.35 mW. Each signal is combined with a CW Laser pump at frequencies of 1330 and 1330.1 nm, with powers ranging from 0 dBm to 10 dBm, through 2x1 WDM multiplexers.

The combined signals enter the Mach-Zehnder interferometer, connected to the 1x2 Power Splitter, with an IIR optical filter at a frequency of 1550 nm between them, where the outputs have FBGs with frequencies equal to 1550 nm. The output signals from the FBGs are coupled back to the Co-Propagating Pump Coupler and passed through the Traveling Wave SOA, as shown in Fig.2. In the receiver, an optical IIR filter at 1550 nm is used to reject interference and noise, before being converted from optical to electrical form by the Optical Receiver, with a cutoff frequency of 0.55 times the Bit Rate in Hz, for a Gaussian Pulse Generator. The output signal is viewed through the Oscilloscope Visualizer and analyzed with the Eye Diagram Analyzed.

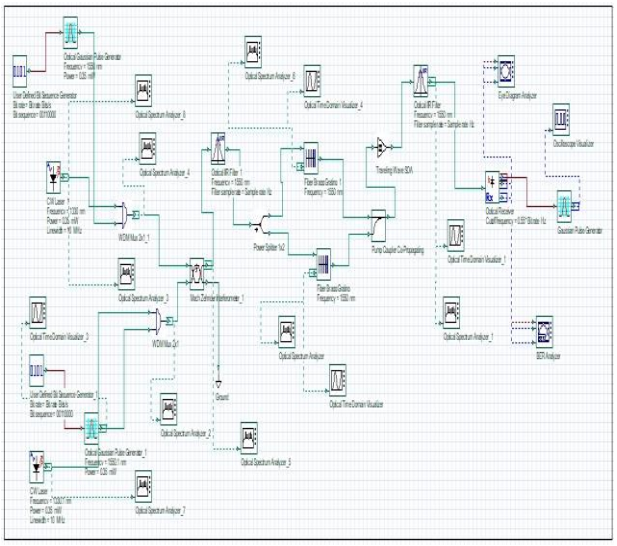

Fig.1. *Overview of the proposed system.*

Table I. *Simulation Results*

Number of Bit	***Input Power***					
	0 dBm		***5 dBm***		***10 dBm***	
	Q-Factor	***BER***	***Q-Factor***	***BER***	***Q-Factor***	***BER***
4	6.00791	$9.290x10^{-10}$	6.00797	$9.286x10^{-10}$	6.00818	$9.274x10^{-10}$
8	11.989	$1.940x10^{-33}$	11.9893	$1.939x10^{-33}$	11.9894	$1.938x10^{-33}$
16	3.57904	0.000168248	3.57906	0.000168233	3.57914	0.000168184

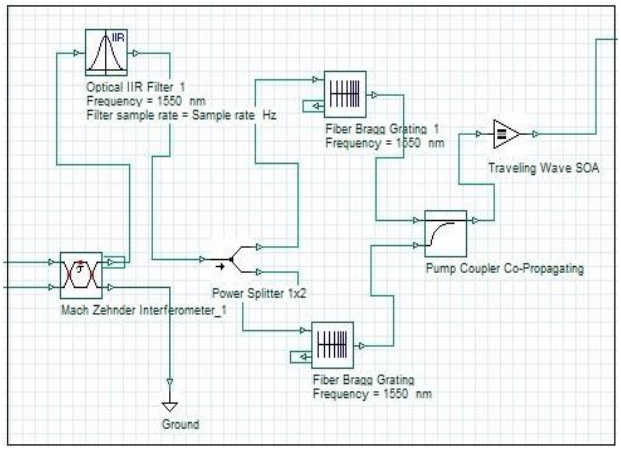

Fig.2. *Mach-Zehnder interferometer combined with SOA and Fiber Bragg Grating (FBG).*

4. Results and Analysis of the Simulations

Table 1 shows the Q Factor and minimum BER for different bit inputs and power of CW Lasers pumps from 0 to 10 dBm. Evaluation of the above results reveals a marked change in the Q-Factor and BER values in response to the variation in the bit sequence transmitted through the proposed communication system. In contrast, the change in power of CW Lasers is practically imperceptible.

Furthermore, it is noted that the most favorable results for the analyzed performance parameters were observed in an eight-bit sequence and an input power of 10 dBm. Figures 3 and 4 show the results obtained using the Oscilloscope Visualizer and the EyeDiagram Analyzer for the 8-bit sequence with an input power of 10 dBm, as they presented the best results among the simulations.

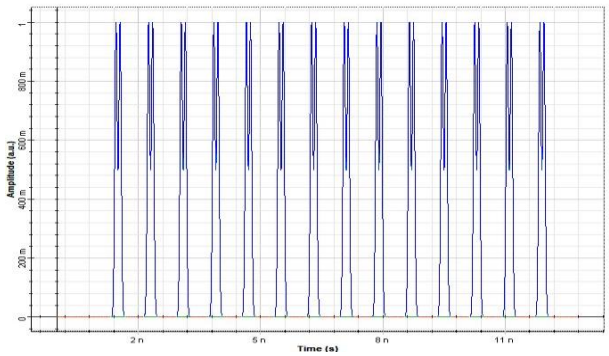

Fig.3 *Output signal viewed on the oscilloscope.*

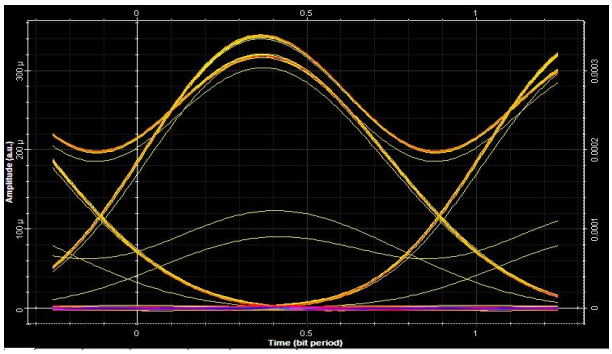

Fig.4 *Eye diagram for an 8-bit sequence and 10 dBm input power.*

4. Conclusions

In this work, we present a system for optical communication that combines the Mach-Zehnder interferometer (MZI), the semiconductor optical amplifier (SOA) and Bragg grating fibers (FBG). The system was simulated and studied using the OptiSystem software. Furthermore, the Q-Factor and bit error rate (BER) were analyzed for different bit sequences (4,8 and 16) and input power (0, 5 and 10 dBm). The results obtained showed a significant variation for the parameters analyzed for the variation of the bit sequence, presenting the best values for an 8-bit sequence with an input power of 10 dBm.

Acknowledgments

This study was financed by the Conselho Nacional de Desenvolvimento Científico e Tecnológico - Brasil (CNPq).

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Analysis of Results of Different Types of Mobility in AlGaN/GaN HEMTs Transistors

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1. Abstract

This work deals with comparing results of different charge mobility extraction methods in AlGaN/GaN HEMT devices. They are field effect mobility (μ_{FE}), effective mobility (μ_{eff}) and low field mobility (μ_0), varying the channel width (W) and gate voltage (V_g). The objective was to elucidate the reasons why μ_{eff} greatly exceeds the values of μ_{FE} and μ_0. Furthermore, the available data allowed the examination of figures of merit for the drain current (I_d), output conductance (g_d) and transconductance (g_m), as well as the analysis of the behavior of the series resistance (R_{SD}), threshold voltage (V_T) and subliminal inclination.

2. Introduction

High electron mobility transistors (HEMTs) have advantageous characteristics, such as superior electron transport, ensuring high speed and better power density [1-2].

HEMT can be understood as a voltage-controlled current source, in which small variations in gate voltage cause large changes in drain current. Therefore, the possibility of accommodating a high carrier density in a two-dimensional electron gas (the 2-DEG channel), i.e. in an extremely thin region very close to the gate electrode, guarantees excellent electronic transport properties, due to the reduction of the interaction between carriers and donor atoms [1-3].

A. Effective mobility method (μ_{eff})

It is considered a gradual channel approximation method as it is based on conduction layer (2DEG) separation between source and drain. In equation (1) the expression for the calculation of mobility is presented [4].

$$\mu_{eff} = \frac{n_G}{C_d(\frac{1}{g_D}-(R_{S-0}n_S+R_{S-0}n_D+R_{S-C}n_C))(V_G-R_{S-0}n_SI_D-V_T)} \quad (1)$$

where C_d-Electrical capacitance per unit area, R_{S-0}-Constant sheet resistance, R_{S-C}-Resistance of sheet contacts, n_C, n_D, n_S and n_G are effective numbers of squares for the ohmic contact, drain, source and gate regions respectively.

B. Field effect mobility method (μ_{FE})

In order to eliminate the impact of the threshold voltage value on the mobility, the transconductance is obtained and substituted in (2) to obtain μ_{FE} [4].

$$\mu_{FE} = \frac{n_G V_{DS}}{C_d(\frac{1}{g_m}-R_{s-0}n_S)(V_{DS}-(R_{s-0}n_S+R_{s-0}n_D+R_{s-c}n_C)I_D)^2} \quad (2)$$

C. Low field mobility method (μ_0)

As in (3), this method allows the extraction of (μ_0) in field effect transistors through the linear approximation for drain current (I_D) versus gate-source voltage (V_G) [4]. Where LG is the channel length under the gate.

$$\mu_0 = S(1 - R_{SD}V_{DS}S)^{-1}(C_dW/L_G)^{-1} \quad (3)$$

3. Device Studied

The HEMT under study is constituted by a substrate of high resistivity of Si <111>, 2 µm of buffer layer (GaN/AlGaN). Its channel is a 300 nm GaN layer beneath a 1 nm AlN spacer that improves density, mobility and drain current. The device also contains a 15 nm barrier of $Al_{0,25}Ga_{0.75}N$ where 0.25 is the molar fraction of aluminum and 0.75 is Gallium molar fraction. A Si_3N_4 cap and SiO as material thickness is added between the 2DEG and the gate metal [4].

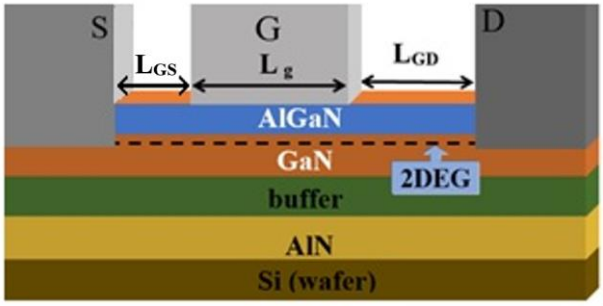

Fig. 1. Illustration of the HEMT structure.

Initially, the drain current values for $V_{DS} = 0.05V$ and for $V_g = 0.2V$ were extracted in the characteristic curves I_dxV_g and I_dxV_{ds} for different values of W, shown in Fig. 2 and Fig. 3 respectively. The same procedure was carried out to extract the current variation as a function of V_g.

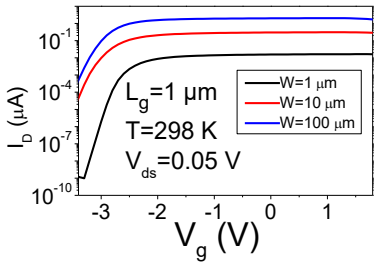

Fig. 2. $I_D x V_g$ curves for $V_{DS} = 0.05V$ With W variation.

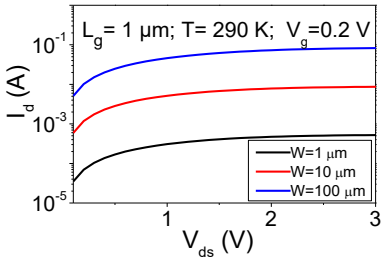

Fig. 3. $I_D x V_{DS}$ curves for $V_g = 0.2V$ With W variation

4. Results and Discussion

In Fig. 2 and Fig. 3 allow us to observe the increase in I_d the greater the V_g and W, because unlike L_g, the greater W offers less R_{SD} to the passage of electrons. These figures also allowed the obtaining of the g_m and g_D curves with their respective values, as well as the extraction of other parameters observed in table I. In relation to V_g, when it is high, the electron gas layer is attracted closer from the gate, which increases the electron density by 2DEG and as a result more electrons move to the drain, increasing I_d.

Table I. *Main parameters for mobility extraction*

W $10^{-6}m$	V_T V	g_D $10^{-4}S$	g_m $10^{-6}S$	R_{SD} $10^{3}\Omega$	I_D $10^{-5}A$	S mV/dec
1	-2.6	3.33	0.91	1.5	1.6	100
10	-3.0	3.45	1.83	0.17	1.8	90
100	-3.1	4.72	1.99	0.025	2.3	80

It was found in this research that regardless of the variable parameter, $\mu_{eff} > \mu_{FE} > \mu_0$ as shown in Fig. 4 and Fig. 5. It can be considered that this result was obtained because it is a semiconductor material that has a high charge carrier density (such as metals), because in these materials electrons or holes are more likely to interact with each other, thus generating relatively greater effective mobility. And μ_0 is smaller, because in low electric fields electrons are more susceptible when they are dispersed by impurities, defects and other imperfections in the material, which limits their mobility [2].

In devices with a short channel (HEMT up to 1 μm), the electric field applied to the gate extends to the drain region, which increases the carrier speed and, consequently, the μ_{eff}. This result is not considered in mobilities that assume a uniform electric field along the channel such as μ_{FE} and μ_0 [2].

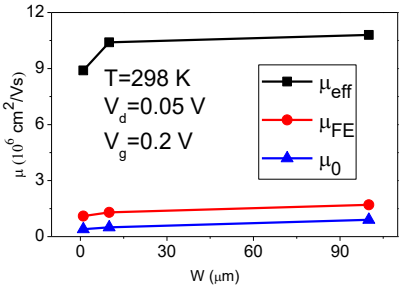

Fig. 4. Extraction of μ_{eff},μ_{FE} and μ_0 with W variation.

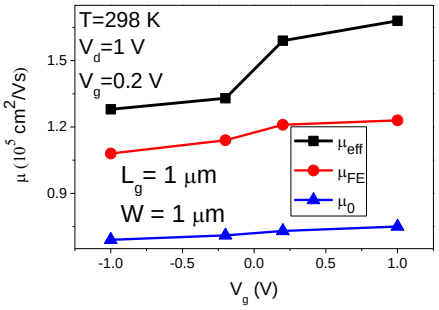

Fig. 5. Extraction of μ_{eff},μ_{FE} and μ_0 with V_g variation.

5. Conclusions

It is possible to verify that the μ_{FE} and μ_0 methods present similar results, while the μ_{eff} method presents relatively discordant results. These differences are explained by short channel effects and modulation of carrier concentration.

Acknowledgments

The authors would like to thank the imec partner program in imec high-speed analog and RF devices and the ARF team for providing the samples. Thanks also to the Brazilian research-funding agency CAPES, FAPESP (Process Nº: 2023/00123-7) and CAADI (Coordination of Affirmative Actions, Diversity and Equity) for supporting the development of this work.

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TCAD-Based Junctionless ISFET Sensing Layers Study

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1. Abstract

This paper shows the sensitivity of JL ISFET with different sensing layers with assistance of TCAD bidimensional simulations. With TiO_2 layer on JL ISFET, the sensitivity increased 12,1% compared to standard SiO_2 sensing layer in all TiO_2 layer thickness simulated.

2. Introduction

The detection of particles, such as ions and molecules, is an important part in electrochemical and biological applications [1]. To detect these particles, the potential difference between two electrodes was registered. Bergveld demonstrated a transistor that detects ions, the Ion Sensitive FET (ISFET), with detects the ions in an aqueous solution [2]. It works with the gate metal removed from a MOSFET device and an aqueous solution with a reference electrode inserted [3]. The ions from the solution bind with the gate oxide (that work as a sensitive layer), affecting the device surface potential, and making the ISFET sensitive to pH [4]. Many biosensors are based on ISFET for detecting DNA, protein, viruses, etc. [5]. These sensors are compatible with MOS technology and can be integrated into the same substrate, allowing to integration of read-out circuits together [3].

Proposed as an alternative solution for the sub–20nm era, Junctionless (JL) transistors aim to simplify the fabrication process [6]. Featuring a constant doping profile from source to drain, JLs contribute to the efficiency of manufacturing. The off state in JLs is achieved by fully depleting the silicon layer on the channel, influenced by the workfunction difference between the gate and the silicon film. In the context of an n-type JNT, an increase in gate voltage reduces the depletion depth, providing a neutral path for current flow between source and drain (I_{DS}). Beyond the flatband voltage, further elevation of the gate voltage (V_{GS}) introduces an additional current component associated with the interface's accumulation layer.

In this paper, the sensitivity of JL ISFET is shown with different sensitive layers through simulations with TCAD Sentaurus tool.

3. Methodology

Sentaurus TCAD [7] is utilized for simulating the ISFET. Notably, the default models in TCAD lack the necessary components to simulate the electrochemical processes inherent in ISFET operation. To address this shortfall, two models are introduced into TCAD through the Physical Model Interface (PMI). These models compute the electrolyte effective density of states and incorporate chemical reactions at the solution/gate dielectric interface via a site-binding model. Furthermore, a Stern layer is integrated to counteract steric effects. These implementations follow the methodology proposed by Bandiziol [8]. Fig. 1 visually represents the simulated cross-section of the JL ISFET.

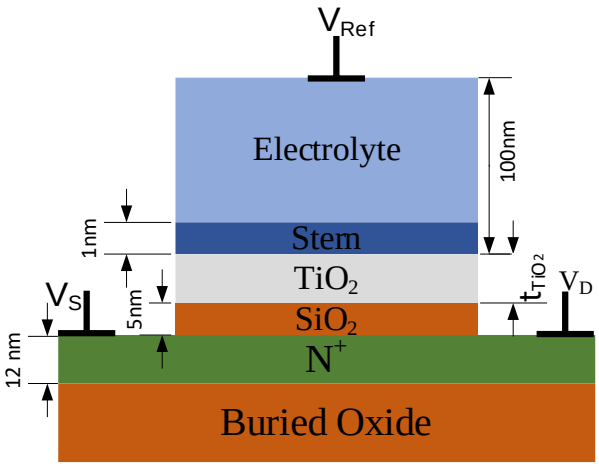

Fig. 1. *Simulated JL ISFET schematic*

3. Results

The JL ISFET is simulated on 20nm SiO_2 Buried Oxide (BOX). Channel length is 200nm and source/drain is 50nm. The Stern layer thickness is 1nm and the electrolyte thickness is 100nm. IALMob and HighFieldSaturation is used as mobility models.

The simulation utilized a SiO_2 and TiO_2 sensitive layer deposited above SiO_2. The SiO_2 layer is 5 nm thick. The silicon film thickness is set at 12nm to achieve complete depletion of the silicon channel, with a doping concentration of $N_D = 1*10^{18}cm^{-3}$ in a bidimensional simulation.

Fig. 2 displays several I_{DS} x V_{GS} curves. All simulations were conducted with VDS set at 20mV to facilitate the extraction of threshold voltage (V_{Th}). The extraction of all V_{Th} values was carried out using the g_M/I_D method.

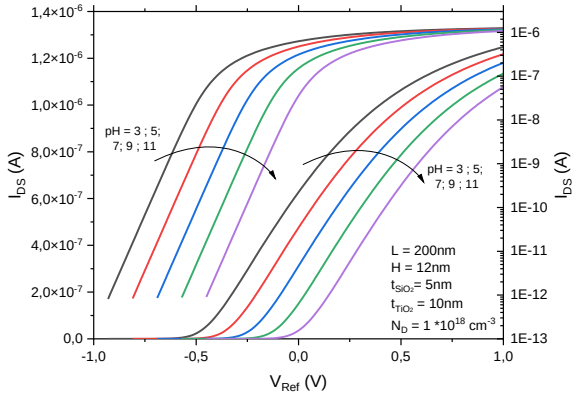

Fig. 2. *I_{DS} versus V_{GS} for various pH values.*

The sensibility of SiO_2 and TiO_2 sensing layers are compared. The structure of ISFET with TiO_2 sensing layer is the same of SiO_2 in Fig. 1, but the TiO_2 layer is placed on top of SiO_2. The sensitivity along the pH range is represented by the ΔV_{Th} x pH, as shown in Fig. 3.

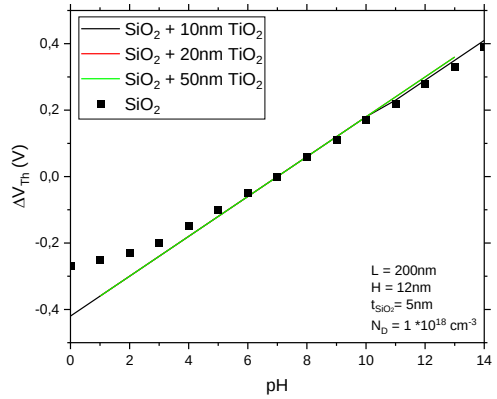

Fig. 3. *V_{Th} variation versus pH.*

The extracted sensitivity of JL ISFET with SiO2 sensing layer is ΔV_{Th} =52,8mV/pH while the ISFET with 10 nm TiO_2 sensing layer showed a sensitivity of ΔV_{Th} = 59,2 mV/pH. This represents an increase of 12,1% in sensitivity. Fig. 4 show the *δVTh/δpH*, evidencing the sensitivity difference. Is important to notice the ISFET with 10 nm TiO_2 shows the sensitivity value equal to the Nernstian limit. And sensitivity is maintained with others TiO_2 thickness, with less than 1,4% difference.

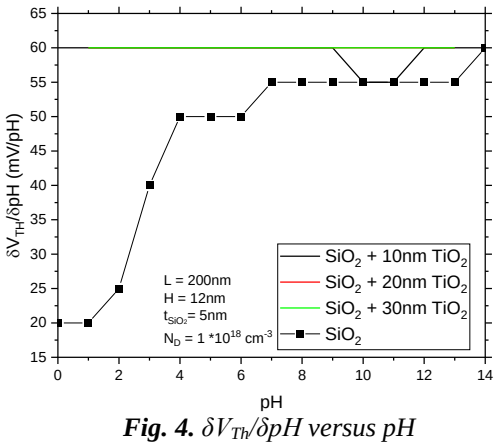

Fig. 4. *$\delta V_{Th}/\delta pH$ versus pH*

4. Conclusions

With the change of sensing layer from SiO_2 to TiO_2, the sensitivity increases by 12,1%. The variation in the TiO_2 thickness negligibly effects the Junctionless ISFET sensitivity, only changing the V_{Th} values itself.

Acknowledgments

The authors of this work would like to thank CNPq for the financial support.

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mmWaves Bias Tee on Metallic Nanowire Membrane

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1. Abstract

With the expansion of communications technologies to mmWaves bands, microwave filters building blocks such as inductive, resistive and capacitive elements require new implementations to address high-frequency parasitics. One of these applications are bias tees which can be implemented off-chip on advanced material interposers using 3D interconnections such as flip-chip and embedded approach to address the challenge. This work presents the current stages of this development at mmWaves Center at USP, with EM simulations indicating promising and high-performance bias tees in mmWaves.

Keywords - mmWaves, bias tee, interdigital capacitor

2. Introduction

The rising need for high data rate communication systems, fueled by IoT, autonomous vehicles, and smart cities, is pushing the advancement of new microtechnologies to enhance bandwidth in the mmWaves range (30-300 GHz). This requires not only novel communication protocols but also a new suite of devices for millimeter-wave transceivers. In microwave systems, capacitors and resistances are for biasing matching networks. However, their development for frequencies like V-band and beyond faces challenges due to significant parasitic effects at higher frequencies. To address this, we propose integrating bias tees on MnM for potential integration with mmWaves transistors for power amplifier development, particularly due to the absence of bias tees on system-in-package (SiP) for high-performance interposer substrates.

3. mmWave Bias Tee Implementation

A. Metallic-nanowire-Membrane

Many PA circuits in mmWaves are still realized through MMICs using CMOS and III-V materials [1]. However, CMOS presents high substrate losses due to Si low resistivity, and while GaAs and HR-Si offer excellent electrical performance, they entail higher costs and in addition MMICs may encounter delays in market entry due to complex fabrication processes. Alternatively, commercial lumped-element are feasible but may limit designer flexibility.

SiP emerges as a viable alternative to MMIC for mmWaves systems, integrating devices from diverse technologies like CMOS for actives and innovative interposer materials for passives. Interposers play a crucial role, routing signals and integrating system modules through interconnects, and can also serve as the main substrate for some devices.

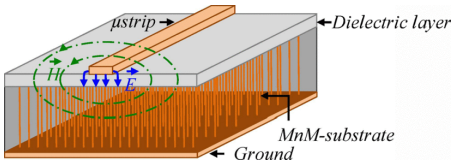

Fig.1. *MnM concept with nanowires grown and its effect on E-field. From [2].*

The metallic nanowire membrane (MnM) shown in Fig. 1 developed at mmWaves Center exhibits superior electrical properties [3], facilitating easy transitions to μStrip-CPW and integration of 3D components like capacitors and inductors. MnM substrate also enables passive miniaturization via controlled slow-wave structure behavior and increased capacitance of the characteristic transmission line as shown also in Fig.1.

B. Bias Tee Design

Interdigitated Capacitors (IDCs) offer simplified single-layer fabrication without wirebonding or interconnects. This characteristic eliminates high inductance common in mmWave applications. IDCs design must be carefully driven in mmWaves and the increasing number of fingers or length can often lead to the appearance of undesired resonances due to parasitic coupling as observed in [4]. Therefore, a parametric analysis is run to observe the IDC behavior by varying its four main parameters: finger length (L) and width (W), gap between them (G) and number of fingers (N). The final design includes the following parameters:

Table I. *Design parameters of IDC structures for millimetre waves.*

Bandwidth (GHz)	Length (μm)	Width (μm)	Gap (μm)	N
40 - 80	175	10	10	3
80 - 150	325			
140 - 220	625			

Smaller G increase capacitance, allowing for L and N reduction for miniaturization, constrained by a 10 μm photolithography limit. Setting width equal to gap optimizes capacitance per unit area [5], while L is tailored to desired operational bands, avoiding unwanted resonances with more than three fingers. As shown in Fig. 2, L is crucial for adjusting bandwidth and self-

resonant frequency due to its significant influence on capacitance. However, increasing L also results in higher inductance as line tracks act as small inductors. Minimum insertion losses were 0.49, 0.63 and 1.11 dB for L = 175, 325 and 625 µm respectively, for N = 3, W = G = 10 µm.

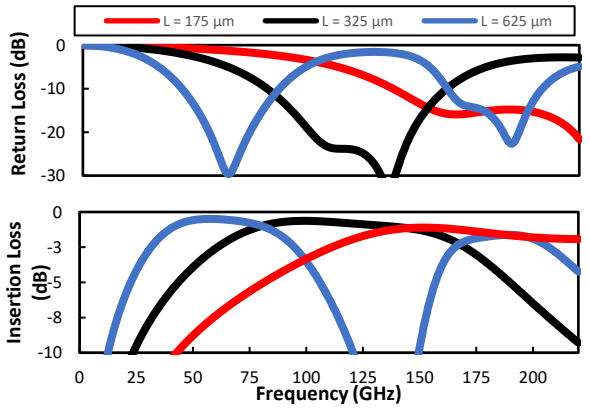

Fig.2. *S-parameters of IDC in a parametric analysis of length.*

The RF-block was designed with a thin high-resistivity Ti film. With a measured ρ between $0.7 \cdot 10^{-6}$ and $2.5 \cdot 10^{-6}$ Ω.m, resistances between 6.7 and 71.3 kΩ were designed with widths of 10, 20 and 30 µm and length 285 µm. The simulated S_{21} or transmission between DC and RF sources is below -40 dB for all cases, which is considered low enough to avoid interference between DC and RF sources. In Fig. 3, it is shown that the electrical field couples between fingers, but not across the resistance in ADS MoM simulation.

4. Fabrication and Integration

Fabrication process involves photolithography of three layers: (1) vias from GSG pads to ground planes, (2) IDC layer and (3) resistance layer. The workflow involves lithography of four layers: (1) bottom, (2) nanowire vias, (3) top capacitor with Cu further electrodeposition and (4) top resistance with Ti thin film deposition. An image of the top layer is shown in Fig. 4.

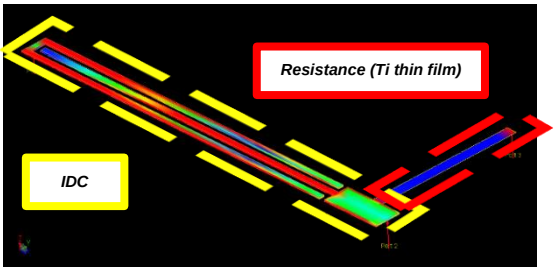

Fig.3. *MoM simulation of bias tee.*

The project aims to enhance fabrication techniques for mmWave interconnections, particularly focusing on flip-chip and planar-level chip integration with suspended CPW lines (PLCi). PLCi involves embedding a CMOS chip into a carrier substrate with the MnM (Fig. 5), ensuring coplanarity and facilitating the fabrication of 10 µm suspended CPW lines with controlled impedance, resulting in improved transition matching and reduced

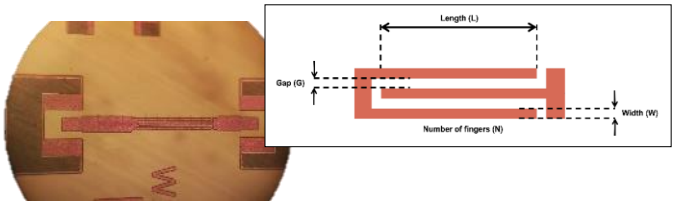

Fig.4. *Top layer IDC after lithography and nanowires on pads.*

inductance compared to wirebonding. Insertion losses in this technique proved to be between 0.4 and 0.7 dB for interconnections between 100 and 500 µm in a recent work from mmWaves Center [6].

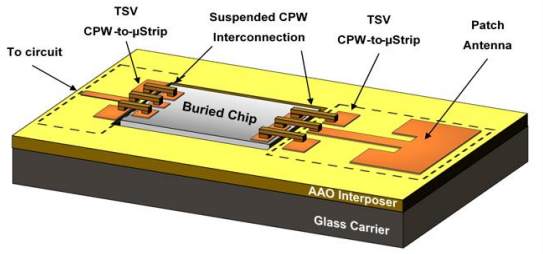

Fig.5. *PLCi and suspended CPW interconnects. From [6].*

5. Conclusions

This study presents mmWaves bias-tees utilizing MnM technology, with simulated IDCs illustrating parameter effects. Miniaturization within photolithography limits optimizes capacitance. Optimization strategies prevent unwanted resonances, while the RF-block guarantees efficient transmisión with insertion loss between 0.5 and 1.1 dB and isolation below -40 dB, supporting high-frequency applications.

Acknowledgments

This work was supported in part by TIMA Laboratory and FAPESP under Grant 2016/25779-9 and 2018/07467-5, CNPq under Grants 309577/2020-9, 311031/2018-8, 431200/2018-1 and 409146/2021-8.

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Exploring Ionizing Radiation and Temperature Impact on pMOSFET Transistors with Varied Layouts

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1. Abstract

This study investigates the effects of ionizing radiation and temperature variations on pMOSFET transistors with two different layouts: ELT and Rectangular. The analysis focuses subthreshold slope and I_{ON}/I_{OFF} ratio to evaluate device robustness. ELT exhibited more consistent responses, suggesting potential resilience to radiation effects.

2. Introduction and Methodology

In electronic devices such as MOSFETs, the effects of ionizing radiation impact their operational characteristics and can cause degradation or even functionality failure [1,2]. Total Ionizing Dose (TID) is cumulative and can affect devices depending on their constructive characteristics.

Ionizing radiation is known for its ability to excite and ionize atoms of the matter it interacts with. Total Ionizing Dose (TID) prompts the creation of electron-hole pairs mainly in oxide regions – those with more structural defects and impurities – leading to an accumulation of positive charges, or trapped holes, in areas such as gate oxide and the Si/SiO_2 interface. This phenomenon, depicted in Figure 1, alters their electrical characteristic [3].

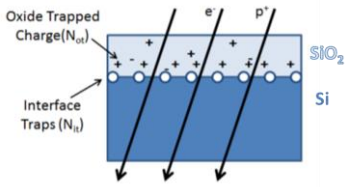

Figure 1 – Formation of positive charges due to TID.

In aerospace applications, electronic systems comprising numerous transistors are highly exposed to ionizing radiation, leading to Total Ionizing Dose (TID) accumulation in these devices. Therefore, it is crucial to consider the radiation-induced effects. Thus, this research aims to evaluate pMOSFET power transistors with ELT (Enclosed Layout Transistor) and Rectangular layouts, having identical channel length and width dimensions, as well as gate oxide thickness. The devices were designed at the Information Technology Center (CTI) using 0.6 µm SOI CMOS technology and manufactured by CEITEC – Brazil.

The ELT geometry aims to mitigate the effects of ionizing radiation by reducing construction imperfections at the oxide interfaces with the transistor's active region, which arise from the manufacturing process [4,5]. In this transistor, the drain or source terminal is surrounded by the transistor's active region, under the gate.

The devices under study were irradiated up to 600 krad with 10 keV x-ray beam and subjected to a temperature test to compare whether, among different device layouts, TID damage could impact the temperature response.

Analyzing post-radiation devices' response to temperature variations is a comparative tool to assess the resilience of various transistor layouts, focusing on parameters like subthreshold slope and I_{ON}/I_{OFF} ratio. The subthreshold slope (S), defined in equation 1, indicates the voltage required to alter output current by 1 decade [2]. A smaller S is preferable, indicating the transistor's ability to switch current levels with lower applied voltage.

$$S = \frac{1}{\frac{\partial \log I_{DS}}{\partial V_{GS}}} = ln\,10\frac{kT}{q}\left(1 + \frac{C_{Si} + C_{it}}{Cox}\right) \quad \text{Equation 1}$$

On the other hand, the I_{ON}/I_{OFF} ratio is related to the gain and power consumption of the transistor [2]. A higher ratio indicates that the off-state current is much lower than the on-current, and energy consumption is reduced for most digital applications.

Following results will show the curves concerning temperature, ranging from 223 K to 353 K. The terms to be presented, "biased mode" and "unbiased mode," mean that the polarization conditions during radiation were different, with the former having an electric field applied by an external voltage and the latter not.

All measurements were conducted with the drain polarized with V_{DS} = -10 mV, varying the gate voltage V_{GS} from 0 to -6 V, measuring drain current I_D (output current). For V_{GS} = 0 V, it was referred to as I_{OFF}, and I_{ON} for V_{GS} = -5 V.

3. Results

For the analysis of the subthreshold slope, the range of interest concerns temperatures above 300 K, where it is possible to observe the effects more clearly since one consequence of temperature increase is a higher thermal generation of pairs [3,5], typically increasing current, with more pronounced outcomes.

By examining the plotted curves below and their corresponding linear adjustments, it becomes evident that only the rectangular pMOSFET exhibited distinct behavior, displaying a more significant variation when subjected to polarization during irradiation (see Figures 2 and 3).

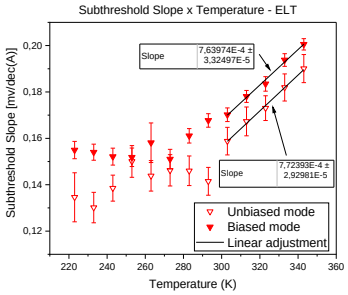

Figure 2 – Subthreshold slope versus temperature in the ELT

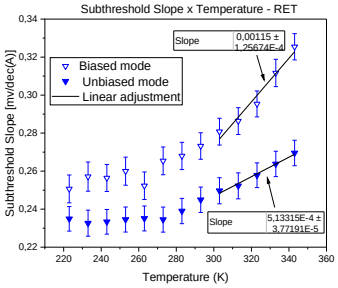

Figure 3 – Subthreshold slope versus temperature in the RET

Conversely, for the ELT, irrespective of the presence of an applied electric field during irradiation (due to polarization on biased mode), the response to temperature effects remained consistent, as indicated by the parallel lines in Figure 2.

Charges generated during radiation exposure, when weakly trapped, are more influenced by the electric field, which was much more pronounced in the rectangular layout compared to the ELT. This indicates that the rectangular layout is more susceptible to the electric field and radiation, as both devices received the same radiation dose. Imperfections in oxide growth in layouts where the isolation between source/drain and gate is worse, are susceptible to retaining more charges, a vulnerability that ELT tends to be more resilient.

Figure 4 shows I_{ON} and I_{OFF} curves for ELT and Rectangular devices in biased and unbiased modes. The primary effect that can be observed is that the presence of field (polarization) during irradiation made the devices more susceptible to the effects of TID, as in both cases I_{ON} current is almost 1 decade lower in the biased mode compared to the unbiased mode.

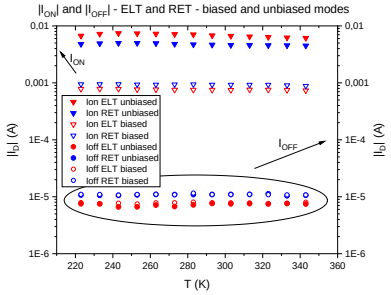

Figure 4 – I_{ON} and I_{OFF} for all modes and layouts

Moreover, consistent with expectations for this geometry, the ELT demonstrates a marginally lower I_{OFF} than the rectangular one. The enclosed geometry proves advantageous by circumventing the "bird's beak" phenomenon inherent in the rectangular layout, a byproduct of the fabrication process.

Notably, when computing the I_{ON}/I_{OFF} ratio, the ELT unbiased mode scenario emerges with elevated values, as depicted in Figure 5, signifying enhanced gain and diminished energy consumption.

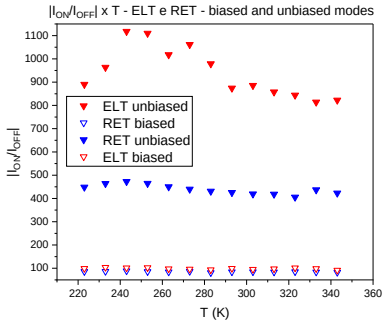

Figure 5 – I_{ON}/I_{OFF} ratio versus temperature

4. Conclusions

Biasing during radiation adversely affects the subthreshold slope response to temperature. Only the ELT layout shape demonstrated insensitivity to polarization during radiation exposure when utilizing this parameter to assess radiation resilience. One possible explanation is that the rectangular layout accumulated a higher concentration of mobile charges than the ELT, thereby exhibiting a greater impact on the applied field. The enclosed ELT layout showcased superior resistance to the deleterious effects of radiation.

The I_{OFF} current of the ELT was expected be significantly lower than that the rectangular layout since it reduces the known effect of parasitic transistors. However, under the conditions of this study, one of the reasons why this difference was not remarkable is because the devices are power transistors and, consequently, have larger dimensions, supporting high voltages. This results in a lower current density that can reduce sensitivity to effects such as variations in I_{OFF} current.

The observation that the I_{ON} in the ELT was more impacted than in the rectangular layout when subjected to polarization during radiation might be a unique characteristic of this device type. Further exploration of additional parameters is warranted to formulate a conclusive hypothesis.

Acknowledgments

The authors acknowledge financial support from the funding agencies. FAPESP. Brazil 2022/09131-0, 2018/25225-9, 2020/04867-2, 2019/07764-1; CITAR: Proc. 01.12.0224.00; INCTFNA, Proc. 464898/2014-5; CNPq: 408800/2021-6, 301576/2022-0, 30360/2020-9.

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Sensor and Circuit Study for an Instrumented Orthosis

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1. Abstract

There is a need for remote monitoring and assessment of hand function during rehabilitation, and this work is part of the development of an instrumental orthosis for this purpose. Specifically, this work presents the study of the Force Sensor Resistor (FSR). Two conditioning circuits were investigated. Results showed the sensor's repeatability and linear behavior after 200g with the current-voltage converter circuit, demonstrating its feasibility for the proposed application.

2. Introduction

One of the frequent and urgent problems worldwide is hand rehabilitation since the lack of hand function has drastic consequences for the individual's daily activities performance, independence, and self-esteem. Robotic devices that can detect and analyze hand efforts have the potential to improve adherence to therapeutic treatment, increasing the effectiveness of rehabilitation. The most recent solutions involve virtual reality systems, exoskeletons, and sensory gloves, in which force sensing resistors (FSRs) and flexion sensors (Flex sensors) have been widely used [1-3].

This work is part of an instrumented orthosis project to enable healthcare professionals to achieve remote hand rehabilitation monitoring due to an instrumented orthosis. Specifically, it aims to conduct the Force Sensor Resistor (FSR) study and propose the circuit for signal processing.

3. Force Sensor Resistor

The FSR is a resistive sensor, which presents a resistance variation proportional to the applied force, showing, a decreasing resistance variation with increasing applied force on a scale of 1/R [4].

The most common technology consists of two layers of semiconductor material printed on a flexible substrate; one homogeneous and the other with interdigitating electrodes. When the two layers are compressed, the connection of the traces increases, reducing their resistance [4].

Two conditioning circuits appear prominently in the manufacturers' manuals. One is a voltage divider coupled to an operational amplifier in a buffer configuration, enabling the adjustment of the system's sensitivity due to RM value but presenting a non-linear output voltage (Fig. 1). The other is a current-to-voltage converter circuit that offers a linear response from 100 g of applied force (Fig. 2) where *Vout* is defined by (1).

$$Vout = Vref \times (RG/R_{FSR}) \quad (1)$$

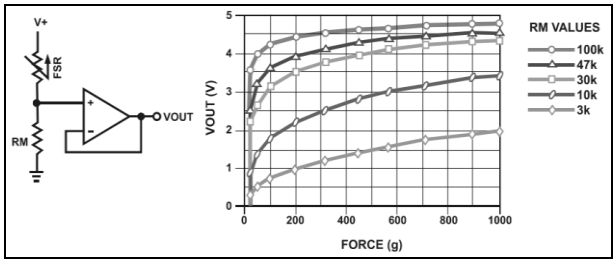

Fig.1. *Voltage divider coupled to an operational amplifier in a buffer configuration circuit* [4].

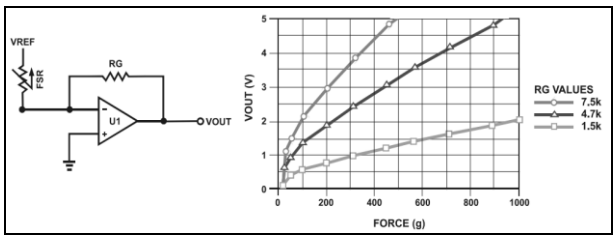

Fig.2. *Current-to-voltage converter circuit* [4].

4. Materials and Methods

The FSR study consisted of two phases: obtaining the sensor's characteristic curve and the output curves of the circuits mentioned in Section 2 with R of 1.5k, 3.3k, and 10k Ohms, Vref=5V and LM358.

An ABS 3D-printed dome was attached to the FSR's sensing area, ensuring a uniform force distribution. Furthermore, a weight kit (Fig. 3) was used, covering a range from 0 to 1kg, based on the representation of the range of force exerted by the human hand during everyday activities.

During the experiments, the sensor was positioned on a support printed in 3D with ABS, enabling the arrangement of weights and uniform transmission of force (Fig. 3).

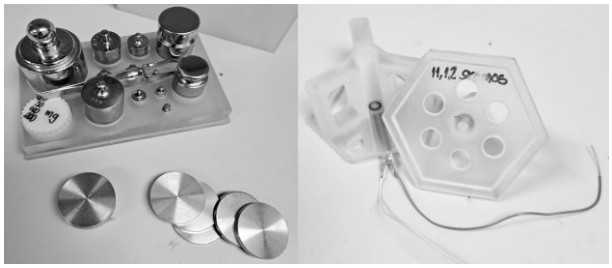

Fig.3. *Weight kit and sensor support.*

5. Results and Discussion

Fig. 4 shows the variation in sensor resistance as a function of force. On the linear scale, the resistance variation can be better described by a power-type equation, while considering a logarithmic scale, the variation is close to linear. This behavior was described in [4], although the values obtained differed. This may partly be related to varying forces using the weight kit. A machine with resolution and precision in the application range was not found. On the other hand, this demonstrates the need to calibrate each sensor.

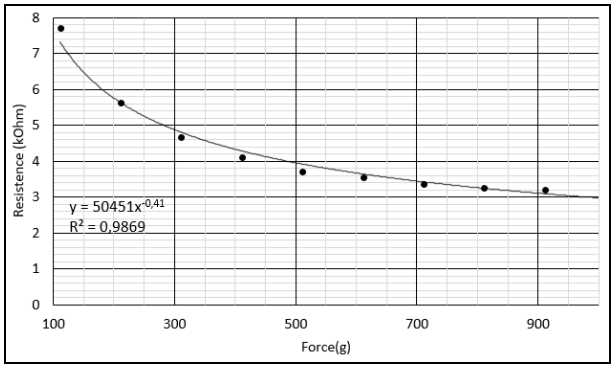

Fig.4. *FSR resistance variation.*

The voltage divider circuit outputs, shown in Fig. 5 and Fig. 6, align with the expectations observed in Fig. 1. As indicated by [4], measurements below 100g are inaccurate. Still above this range, the curves showed a non-linear voltage increase with the applied force. Sensor presented reasonable repeatability for 3 measurement trials, with deviations better than 8%.

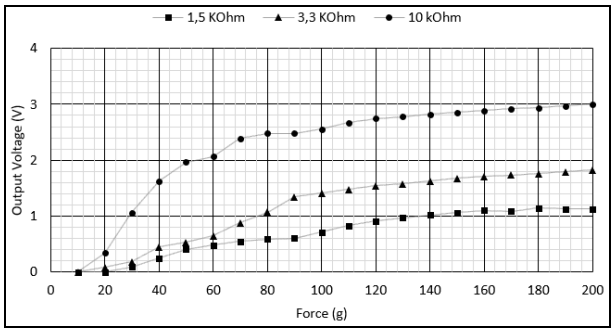

Fig.5. *Voltage divider circuit output.*

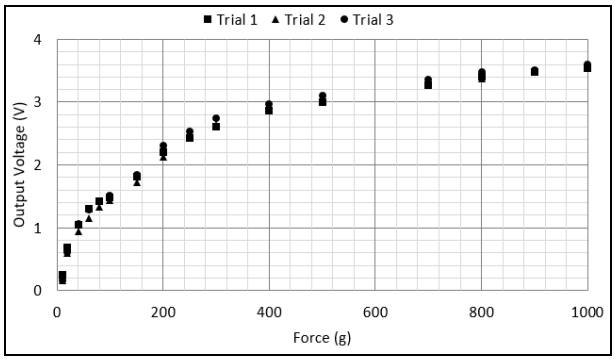

Fig.6. *System repeatability.*

Fig. 7 shows the output variation for the current-to-voltage converter circuit with R_G=3,3k Ohms. Although the entire curve can be adjusted by a ln-type curve fit, starting from a force equal to 200g, the behavior is closer to linear, as expected. However, for a better resolution, a higher RG should be used.

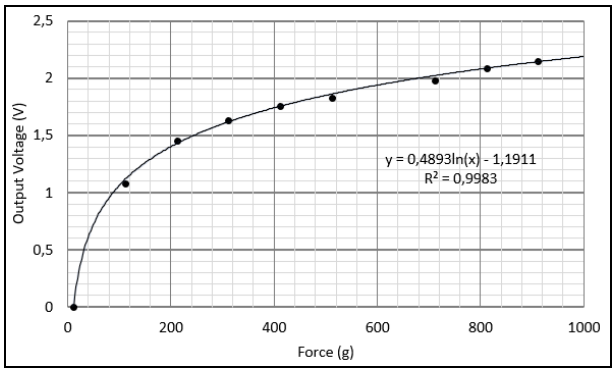

Fig.7. *Current-to-voltage converter circuit output voltage.*

6. Conclusions

The FSR study results demonstrated its feasibility for force monitoring. Highlighting the repeatability of the sensors, and the linear behavior after 200g with the current-voltage converter circuit.

Acknowledgments

The authors thank FEI and FINEP for their support.

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Tantalum Ultrathin Films for Silicon Carbide Schottky Barrier Diode

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1. Abstract

Since their first studies, ultrathin films investigated in silicon carbide (SiC) Schottky barrier diode (SBD) with refractory metals has been exhibited levels of Schottky Barrier heights (SBH) related low power consumption and could provide high thermal stability. To include another metal to the list of refractory metals, tantalum was chosen to present some primary results about such structure and features performance under different annealing treatments. In the first results, values of SBH about 0.7 eV and leakage current under reversed bias around micro amps were obtained.

2. Introduction

The first device based on SiC released was a Schottky barrier diode (SBD), and device is basically a junction of a semiconductor and a particular metal capable of providing a rectifier contact. Theoretically, considering a n-type semiconductor, the rectifying event occurs when the metal to be joined presents work function higher than the electron affinity of the semiconductor, and hence, the difference of them yields a Schottky barrier heigh (SBH) in electron-volt units [1]. However, in practical analyses, the results show some deviations, in that case, remaining open issues to be investigated and provide a comprehensive agreement [2]. It is important to mention that until this publication, there is no stablished nor fully understanding regarding about the difference between theorical and practical, furthermore, this issue is beyond the purpose of this work and these events are further discussed in other publication [3]. This lack, meanwhile, generates the purpose for researching, in this case towards of the development of SBH with addressed values, i. e. values according to the design and purpose desired. So then, in different circumstances, the production would barely just be choosing the metal and joined with the semiconductor.

In this scenario, now a days, instead just the work function of the elements, by choosing different metals, the relation with the surface conditions brings a substantial impact, leading to more comprehensive approach about the properties of Schottky contacts, improvements and tunning in SBH, leading to research and production [4]. Once the surface aspects are interest for engineering the SBH, it is also important to pay attention at quality of the interface between metal and semiconductor, e.g., inhomogeneous levels, defects, impurities, and morphology, which can cause interface states and shifts the ideality factor far from nearly 1 [5]. Since then, forms to perform surface arrangements associated with best quality has been employed, being metallization techniques, annealing treatments[6], types of metals [7], alloys [8], surface treatments and cleaning, surface inserts and geometrical arrangements [9], and even the addition of tiny oxides [10],, where some of these applications can tune the values of SBH and improve the results of the reliability features [11]. Besides all the methods of changing the SBD it is worth to mention that the SBH nearly 0.7 eV is ideal for power devices, contributing for low power consumption, whereas values around 1.1 eV or higher are mostly used for high frequency applications [7].

3. Methods and Materials

Initially, a double side polished SiC wafer n-type of 350 µm thick (0.015~0.028 Ω.cm) with drift layer of $3x10^{15}$ cm^{-3} dopants and 30 µm thick was selected. The samples were diced in 1 cm^2 and followed by lithographic pattern with squares of 3 mm side. The samples were cleaned with 10 minutes in piranha bath, followed by 10 minutes immersed in nitric acid 30% at 50 ºC. After the cleaning process the devices were initially fabricated with 2 nm of tantalum deposited by sputtering at the top of the samples to form Schottky contact and then, rapid thermal annealed performed from 500 to 700 °C under 50

°C intervals. To cover the ultrathin film, 100 nm of aluminum was deposited by thermal evaporation to protect the first film and provide electric contact for test probes. To create the ohmic contact, 100 nm of nickel was deposited by sputtering without any thermal treatment. The samples were diced in 1 cm^2 and followed by lithographic pattern with squares of 30 µm side.

4. Results

The devices were verified by IxV curves, performed by Keithley 4200-SCS parameter analyzer. Each device was submitted to IxV curves to check the current response, leakage current under reverse bias, SBH, and ideality factor. At Fig. 1 it is possible to verify that the annealing treatment yielded the difference among the annealing treatments. The best result was related to the 650 ºC which showed a substantial leakage current and value of SBH around 0.74 eV and ideality factor of 1, resulting in a low resistance device addressed to power devices, combined with the lowest leakage current, as shown in Fig. 2.

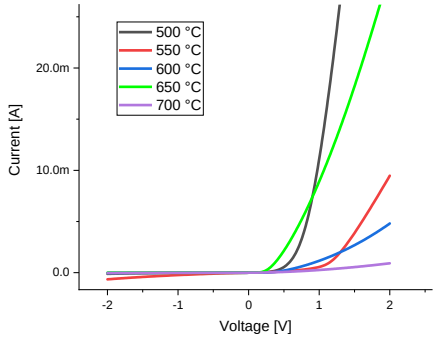

Fig. 1 *– IxV curves of different annealing process.*

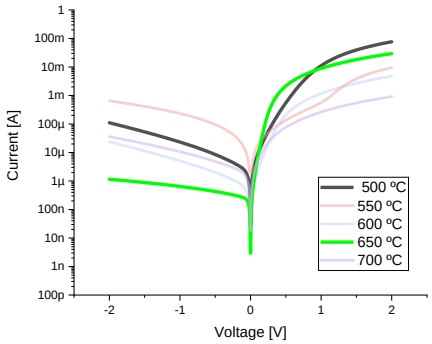

Fig. 2 *– IxV semilog graph of curves under bias and reverse bias.*

4. Conclusion

The results based on an initial approach, showed that the values obtained could provide substantial features about low power consumption, ideality factor and keep the leakage current under micro amperes, which even though without tests performed at higher temperatures, the results could lead to further investigations.

Acknowledgments

The authors do express their compliments to the CCSNANO, CTI and CNPEM laboratories as well as for being supported by their handy team.

The work was supported by SAE UNICAMP and Eldorado.

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Study on Basic Polymer Waveguide Interpose Structures Applied to Photonic Packaging

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1. Abstract

The move from electronic to photonic data processing is not a one-to-one copying process. Optical connections between chips, interposers, and boards are considered a viable alternative for fast data transfer. We are proposing to use polymer waveguides interposer for routings and connections of light-conducting layer. This manuscript presents a numerical study of vertical coupling between SU-8 waveguides that should be performed as interposer in an optical packaging technology under development.

2. Introduction

Optical fiber has been used for long distance transmission, meeting technological and market needs. However, for optical hybridization and short-haul interconnections if adopted the same solution using fiber, there will be a chaos as occurred with electronic devices before the PCB approach, which with complexity of the solutions induced multilayer board evolution. However, the philosophy of electronic processing for photonics is not a simple copy or transportability of concepts. It is necessary to ensure the integration of devices for creating, processing, transmitting and receiving light, as well as electro-optical transceiver and conversion technology, as illustrated in Fig. 1, by combining several techniques [1].

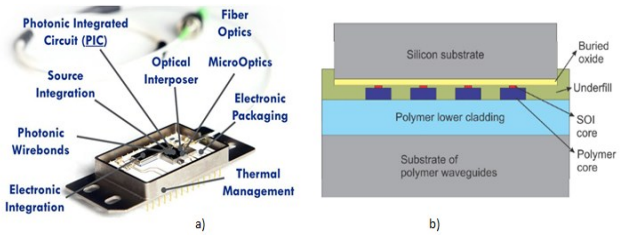

Fig.1. *a) Optical Packaging illustration (source: pixapp.eu) b) Waveguides flipchip connection.*

The range of different photonic integration is wide and is underway [2]. This paper presents optical coupling schemes using polymer waveguides optical for interposer configuration.

3. Optical Interposer Structures

The interposer is an optical interface routing between one layer or connection to another (Fig. 2) [3]. These structures are used to distribute the optical signals, similar to the role played by copper traces and vias in established high-density electrical laminates.

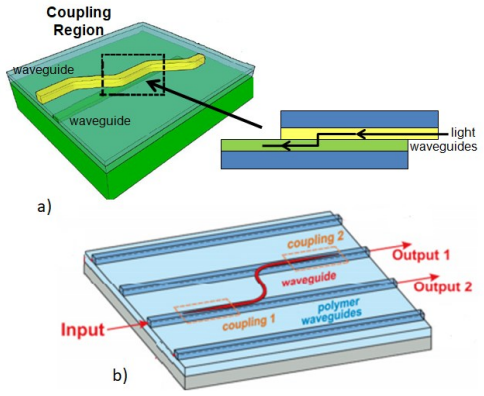

Fig.2. *a) Vertical S-shaped coupling between two waveguides b) example of optical signal routing.*

The study is based on SU-8 waveguides (Fig. 3), once this polymer is widely used as functional structures for 3D micromechanical structures with excellent mechanical characteristics, water impermeability, high stability, high uniformity and chemical resistance. It is also an optically transparent polymer with high refractive index and transmission greater than 95% beyond a wavelength of 400 nm; very suitable for optical solutions.

The interposer structures are supported by two types of SU-8 waveguides developed in previous works [4, 5] - ridge and inverted rib waveguides (see Fig. 3).

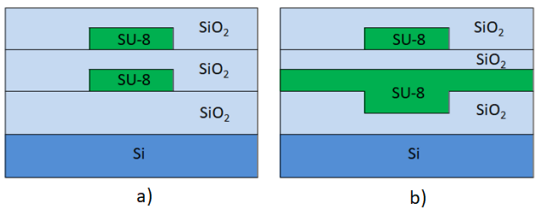

Fig.3*. Interposer - a) ridge/ridge waveguides b) inverted rib/ridge waveguides.*

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4. Results

The vertical coupling in the structures was simulated at λ =1550 nm, for both TE and TM polarization modes (Fig. 4 and Fig. 5), using the commercial package COMSOL Multiphysics - Wave Optics Module. The gap between the two waveguides was defined by the silicon oxide interlayer. The results are summarized as following.

A. Ridge /Ridge Interposer

Waveguide dimensions → 1.7 (W)x1.2 (H) µm;
SiO_2 interlayer thickness → 0.3 µm;
BOX → 4 µm;
SiO_2 cladding → 0.5 µm.

Table I. *Values of Effective indexes and coupling coefficients of both coupled modes @ λ = 1550 nm.*

η_{eff} TE		η_{eff} TM	
Symmetric	Assymetric	Aymmetric	Assymetric
1.514123	1.483045	1.513232	1.480260
κ_{TE} = 0.063		κ_{TM} = 0.066	

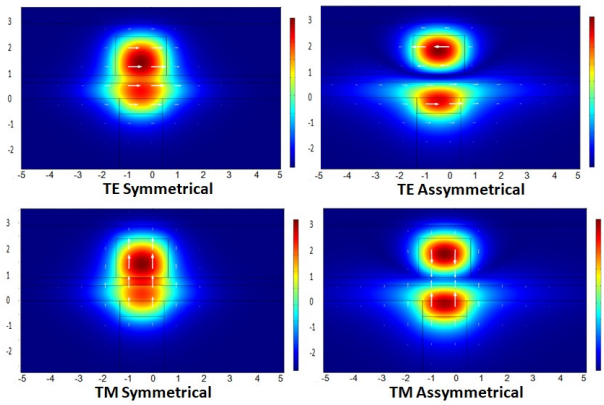

Fig.4. *Simulated normalized field modulus across coupler cross-section - symmetrical and assymmetrical modes.*

B. Inverted rib/Ridge Interposer

Inverted rib:
Waveguide trench dimensions → 1.7 (W)x0.6 (H) µm;
Rib thickness → 0.6 µm;
Ridge:
Waveguide dimensions → 2.0 (W)x1.5 (H) µm;
SiO2 interlayer thickness → 0.3 µm;
BOX → 4 µm;
SiO_2 cladding → 0.5 µm.

Table II. *Values of Effective indexes and coupling coefficients of both coupled modes @ λ = 1550 nm.*

η_{eff} TE		η_{eff} TM	
symmetric	assymetric	symmetric	assymetric
1.526320	1.498737	1.524615	1.495598
κ_{TE} = 0.056		κ_{TM} = 0.059	

Considering the variables n_{eff} and κ shown in the tables I and II, we can define de coupling length L (coupling region) between the waveguides, as ilustrated in the Fig. 2. For interposer structure a) results L = 25 um, and for structure b) L = 30 um.

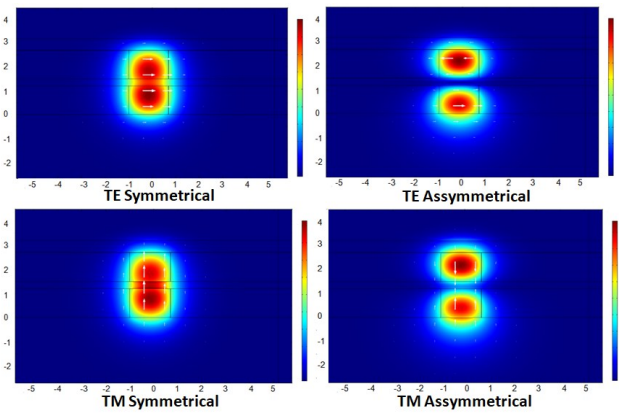

Fig.5. *Simulated normalized field modulus across coupler cross-section - symmetrical and assymmetrical modes.*

5. Conclusions

Some optical interposer structures were proposed demonstrating that they can be used for routings and connections of light-conducting layer. These SU-8 waveguides were already fabricated and tested in some building blocks (DC, MRR, Y-junction, etc), being able to meet the requirements of an interposer for optical packaging.

Acknowledgments

The authors would like to thank the Brazilian Research National Council (CNPq - PCI 444303/2018-9), for financial support and COLAB's technical staff from CTI Renato Archer and Prof. G. Malheiros-Silveira from FEEC/UNICAMP for contributions during this work.

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SiO_2 etching process optimization, for facets formation in photonic chips based on $LiNbO_3$ thin films.

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1. Abstract

In the field of integrated photonics, devices such as waveguides and optical cavities play a fundamental role in manipulating light inside a photonic chip. Therefore, achieving good fiber-to-chip coupling and vice versa is essential for integrating photonic chips into our current optical fiber based telecommunication system. In this work, we present the development of silicon dioxide etched facets aimed at reducing scattering losses during lateral coupling to a photonic chip. This sequence is already used for silicon nitride lateral compiling and will be an important component for manufacturing photonic chips based on lithium niobate ($LiNbO_3$) thin films.

2. Introduction

Photonic integrated circuits (PICs) play a key role in optical interconnections, optical computing, and optical neural networks due to their high speed and low energy consumption. Within this field, lithium niobate ($LiNbO_3$) on insulator, has emerged as one of the most promising platforms for PICs due to its wide transparent window, high electro-optic coefficient, and nonlinear optic behavior. Photonic devices like waveguides and microring resonators are driving the next generation of PICs [1-4]. At the same time, the linking of integrated photonic circuits to off-chip systems, is an essential requirement for the practical use of PICs. External coupling often imposes major limitations on the environmental stability and performance of photonic integrated circuits, especially regarding loss [5, 6]. A good light coupling between the optical fiber and the photonic chip is essential to guarantee the correct functioning, especially in applications very sensitive to losses such as the ones related to quantum information processing and communication.

In this context, the present work introduces a sequence for manufacturing facets with low roughness, greatly limiting losses induced by scattering, using optical lithography and ICP-RIE etching.

3. Experimental Details

The typical starting point of our process will be a thin film stack composed by $LiNbO_3$ (500nm) over silica (2µm) over a silicon substrate (~500µm). However, due to cost considerations, in this study, we used samples of, 2µm SiO_2 layer over Si substrates measuring 10 × 10 mm. We conducted photolithography using a MicroWriter ML3 and photoresists AZ 5214, AZ p4620, and AZ 3312. The most satisfactory results were achieved with AZ 3312, which underwent final adjustments. We performed etching processes using an Oxford ICP-RIE PlasmaLab System 100 available at CCSNano. The manufacturing sequence of the tested samples is illustrated in Fig. 1. We employed etching times of 5, 10, 15, and 20 minutes to determine the etching rates of both the photoresist and the SiO_2 film.

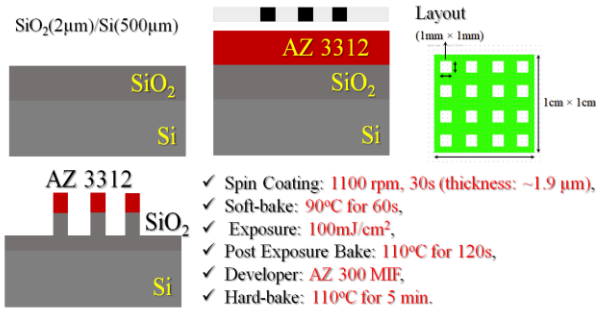

Fig.1. *Manufacturing sequence of the samples used in this study.*

After we manufactured the samples, we used a stylus profilometer (Dektak XT profilometer) to conduct thickness measurements for each etching time. Additionally, we examined the morphology of the facets using optical and electron microscopes (Olympus Mx51 and SEM FEG Mira 3 XMU-Tescan) to assess facet roughness, as this parameter is crucial for determining facet quality.

4. Results and Discussion

From the optical microscopy images shown in Fig. 2, we can observe a well-executed lithography and etching process, where the layout format used before and after etching is maintained.

From the thickness measurements for each etching time, we were able to establish the etching rate of both AZ 3312 and SiO_2, as depicted in Fig. 3. Additionally, good reproducibility in the etching processes and excellent selectivity of the photoresist for this etching recipe were confirmed. The range of colors for the different times corresponds to the thickness of the remaining films after etching. The etching rates were 100nm/min for SiO_2 and 70nm/min for AZ 3312, respectively.

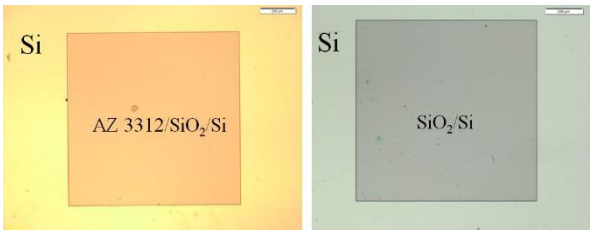

Fig.2. *Left side: optical microscopy image of the lithograph process. Right side: optical microscopy image after 20 min of plasma etching and photoresist removal (recipe: CHF_3/O_2 -52sccm/3sccm, ICP: 1200W, RIE:45W).*

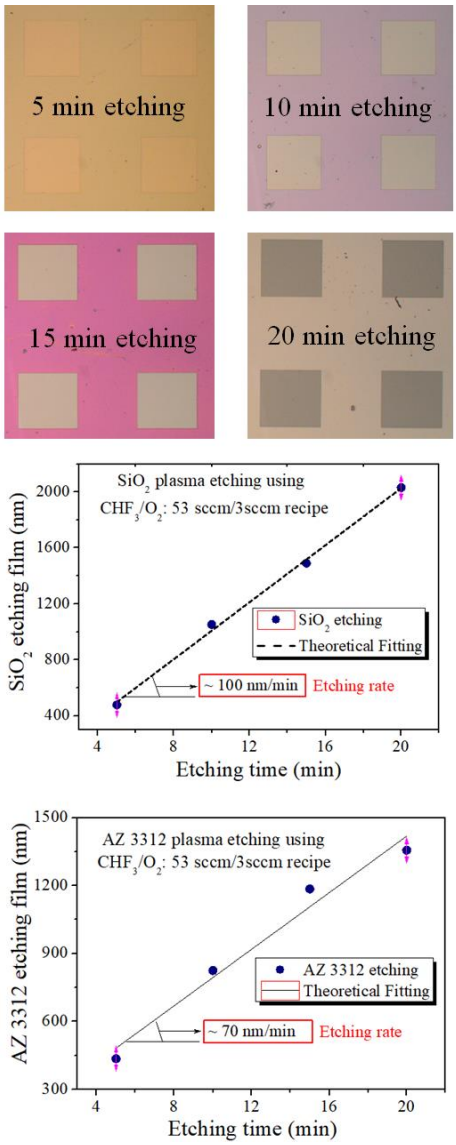

Fig.3. *Upside: optical microscopy image for each etching time. Downside: Etching rate from SiO_2 and photoresist AZ 3312 using a CHF_3/O_2 plasma*

Fig. 4 presents electron microscopy images taken of sample 4 (sample with 20 minutes of etching). These images reveal a low roughness of the facet, allowing us to corroborate its thickness (2µm)

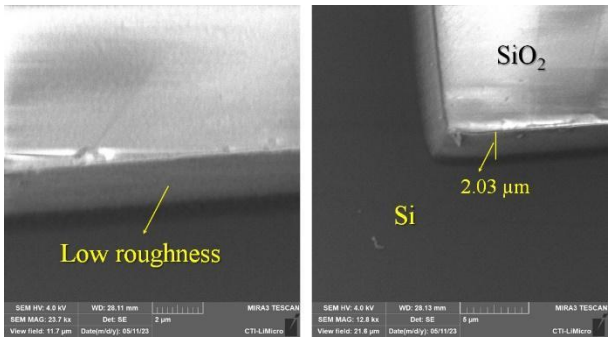

Fig. 4. *SEM imagen from sample 4 (sample with 20 min of etching)*

5. Conclusions

Based on the results obtained in this study, we can conclude that we were able to fabricate silicon dioxide etched facets with high reproducibility and good quality using photolithography and ICP/RIE plasma etching in local cleanroom facilities. The developed recipient will be useful to decrease the scattered light at a photonic chip facet. These findings also indicate that the selected plasma recipe is highly suitable for this particular photoresist.

Acknowledgments

To São Paulo Research Foundation (Fundação de Amparo à Pesquisa do Estado de São Paulo) for the financial support of this research (process: 2022/15141-8, linked to the process: 2018/03474-7). To Assembly, Packaging and System Integration Division from Renato Archer Center for Information Technology, for infrastructure support.

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Characterization of MOS Capacitors on 4H Silicon Carbide Substrate submitted to ionizing radiation.

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1. Abstract

This paper presents a study of the characterization of the MOS capacitors when subjected to ionizing radiation. Such experiments support analyzing the robustness of silicon carbide semiconductor devices, which has attracted increasing attention due to its robustness properties and tolerance to ionizing radiation. For these studies, beta radiation was applied as a source of ionizing radiation, and the Capacitance - Voltage and Current-Voltage characteristics were obtained for devices as-fabricated and post-irradiation. The extracted Flat-band Voltage (VFB) and Leakage Current (LC) parameters were compared to evaluate the irradiation robustness.

2. Introduction

Since the 20th century, silicon carbide has presented a significant increase in interest due to its thermal and electrical properties. Comparative data between silicon (Si) and silicon carbide (SiC) show that factors such as high band gap, high thermal conductivity capacity, high mechanical rigidity, adequate chemical stability, and a high breakdown voltage are superior to the properties of silicon. These properties of silicon carbide give it an exciting future as a material for developing semiconductor devices for high-power and high-temperature applications. Because of its tolerance to harsh environments and ionizing radiation, research has been directed toward developing electronic components with applications in the space segment and sensors for the nuclear reactor industry. [1]. In this context, this work intends to present the first results of irradiation robustness of Metal (Al) –Oxide (SiO2)-Semiconductor (SiC) capacitors under beta exposition. The flat-band voltage (VFB) and leakage current (LC) parameters, which were extracted from C-V and I-V curves, respectively, were compared to evaluate the robustness of irradiation.

3. Experimental Procedure

In our experiments, MOS capacitors were fabricated with 300 nm thick aluminum (Al) upper and down electrodes [2] and 50 nm thick silicon oxide (SiO2) deposited on the N-type 4H-SiC wafers with a 30 µm thick epitaxial layer ($3x10^{15}$ cm^{-3}), and a 350 µm thick substrate ($3x10^{18}$ cm^{-3}).

We carried out the beta irradiation experiment on one sample (post-irradiation). Another control sample (as-fabricated) without irradiation was used to compare the VFB and LC parameters extracted from C-V and I-V curves, respectively. To irradiate the sample, a Strontium 90 was a beta source with an energy of 1955.7 KeV, a dose rate of 566 Rad/hand, and an exposure time of 72 hours. The Capacitance - Voltage and Current-Voltage characteristics were obtained for devices as-fabricated (control) and post-irradiation. The extracted Flat-band Voltage (VFB) and Leakage Current (LC) parameters were compared to evaluate the irradiation robustness.

4. Results and Discussions

The 1MHz Capacitance - Voltage (C-V) and Current-Voltage (I-V) characteristics were obtained for as-fabricated and post-irradiation devices. In both samples, at least five capacitors were measured. Figure 1 presents examples of the C-V curves for as-fabricated and post-irradiation MOS capacitors. To obtain the VFB values, the criteria of 0.65 of maximum capacitance was used. In these cases, the hysteresis in the depletion region for forward and backward curves were not presented. However, the hysteresis were extracted. All curves were normalized, and for the 0.65 point in normalized capacitance, the VFB was extracted.

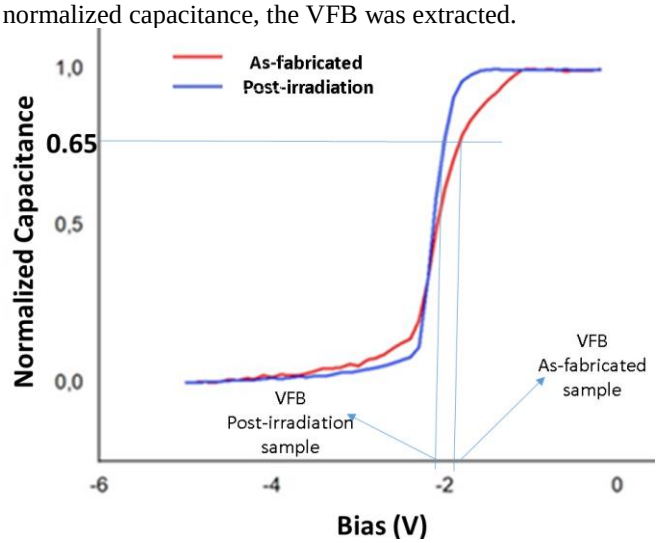

Figure 1 - C-V curves for as-fabricated and post-irradiation MOS capacitors.

The Current-Voltage (I-V) characteristics were obtained for as-fabricated and post-irradiation devices, and the leakage current values were extracted for 2 V, in

the accumulation region bias for each capacitor.

Table 1 presents the average values of VFB and hysteresis, which were extracted from C-V curves, and leakage current for 2V (accumulation region), extracted from I-V curves. The standard deviations were extracted because at least five capacitors were measured for each sample.

Table 1. The average values of VFB and hysteresis, and leakage current for 2V (accumulation region) with the standard deviations.

SiC MOS Devices	VFB (V)	Hysteresis (V)	Leakage Current (μA)
As-fabricated	-2.01±0.13	0.05±0.04	297±34
Post-irradiation	-2.33±0.37	0.36±0.32	201±92

From Table 1, the average values of VFB of -2.01 and -2.33 for as-fabricated and post-irradiation devices were obtained, respectively. If these values are more negative, an increase in effective charge densities at SiO2/SiC structures can be expected after beta irradiation. The difference between them of 0.32 V indicates a 16% charge density increase. The hysteresis values also increased to 0.05 V for 0.36 V, seven times higher. This agrees with the VFB results. Therefore, MOS capacitors are damaged after beta irradiation. However, it can be expected that this damage was not high due to the extracted average values of leakage currents of 297 μA and 201 μA for as-fabricated and post-irradiation devices were obtained, respectively. These values are the same level of magnitude order with a reduction of 32% in the comparison. Thus, our results indicate that the irradiation damage at MOS capacitors on the SiC substrate was not severe. So, SiC devices can be used for applications with irradiation exposure, such as in space aircraft.

5. Conclusions

In this work, beta irradiation was applied as a source of ionizing radiation on SiC MOS devices, and the Capacitance - Voltage and Current-Voltage characteristics were obtained for devices as-fabricated and post-irradiation. The extracted Flat-band Voltage (VFB) and Leakage Current (LC) parameters were compared to evaluate the irradiation robustness. The obtained r results indicate that the irradiation damage at MOS capacitors on the SiC substrate was not severe, and these devices can be used for applications with irradiation exposure, such as in space aircraft.

Acknowledgments

This work has financial support by ROTA 2030 and Softex_MCTI projects, INCT Namitec and CNPq.

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An Internal Clock Family into Low-Cost Cyclone V FPGA for High-Range and High-Resolution TDCs

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1. Abstract

This study aims to describe the design of three internal oscillators on a low-cost FPGA board. These oscillators will serve as the reference time base for counters in TDCs. In this paper, sequential devices were arranged in a delay chain, designed to generate internal frequencies of 250, 500, and 750 MHz. To conduct frequency measurements of these oscillators, in the MHz range, a 13-bit divider was placed internally in the FPGA to get a proportional signal, in the kHz range, connected to an output pin of the FPGA board. The 500 MHz oscillator varied by 1%, while the 750 MHz oscillator increased by 25%. The 250 MHz oscillator showed no signs of testing. Promising results highlight the efforts to develop a clock family suitable for high-range and high-resolution TDC applications.

2. Introduction

The simplest and most reliable element for direct time measurements is the counter. A clock synchronizes the counter on its time base, and this clock defines the resolution and precision that the system will have. The clock from an oscillator is the time base that will allow accurate times to be measured [1].

Researchers have increasingly studied time-to-digital converters (TDCs) with the evolution of technologies. Applications such as autonomous vehicles, particle counting, and topology verification, among others, are real. TDCs measured the difference in time from a signal emitted and reflected with high precision. There is no defined figure of merit (FoM) for TDCs, however, some parameters define their usage characteristics, which are resolution, range, and linearity. A deeper understanding of the topic can be done by searching the references [1, 2, 3, 4, 5, 6]. Figure 1. Illustrates the simplified diagram block proposed.

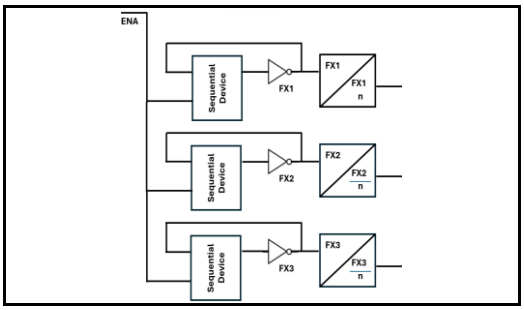

Fig.1. *Simplified block diagram.*

In this work, we aim to use a low-cost Terasic DE10-Nano development kit with 50MHz frequency limitations and develop internal oscillators into the FPGA to prove its functionality by measuring them externally [3].

Therefore, we designed 3 proportional frequency blocks and dividers to reduce them. This allowed to measure them externally using the resources of the two GPIO 40-pin expansion headers [7].

3. Simulation and experimental results

A. Architecture, design, and simulation

This project was designed in portable HDL language sequential devices with an inverter delay chain to get three specific frequencies: 250, 500, and 750 MHz. These frequencies were constrained correctly in a Synopsys Design Constraints file, SDC. Figure 2. illustrates the ModelSim - Intel FPGA Starter Edition 2020.1 simulation. Which comes installed with Quartus Prime Lite 20.1.1.

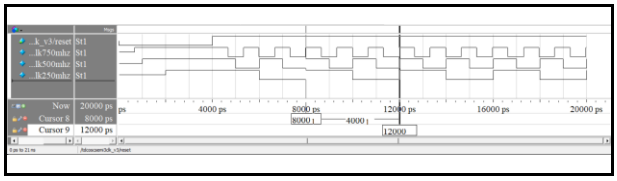

Fig.2. *Simulation of 250, 500, and 750 MHz frequencies.*

To extract the signal generated, we designed a thirteen-bit frequency divider. This device will divide the frequency by 8.192. Assigning to output ports about 30, 60, and 90 kHz. Figure 3. illustrates the simulation of these frequencies at the same simulator described before.

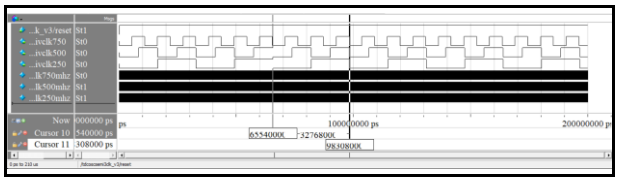

Fig.3. *Simulation of 30, 60, and 90 kHz frequencies.*

B. Environment Testing

The testing environment setup illustrated in Figure 4. includes a bench with a DE10-Nano development board, a computer with Quartus Prime Lite 20.1.1 installed, and an MSO9404 Oscilloscope. In addition, a

set of male/female jumpers to access the GPIO header. This setup allows testing coarse and fine frequencies of TDCs.

Even reducing the number of bits from the divider. The limitation of high frequencies is the GPIO header at 50 MHz. In simplifying testing, we worked in kHz.

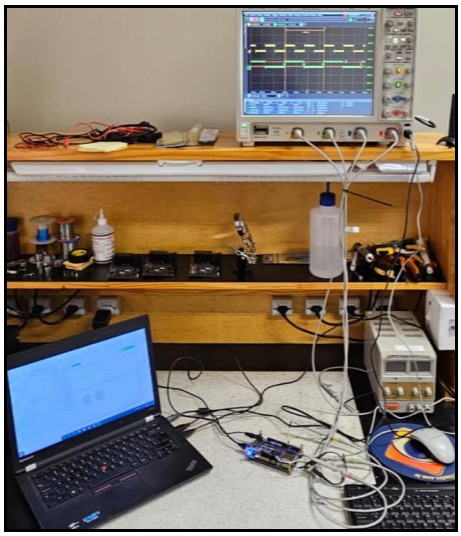

Fig.4. *Test environment of clock family into DE-10 Nano board.*

C. Experimental results and discussions

We designed three internal clocks free of timing analyzer warnings approaching the recommended practices. The divider reduces the three-megahertz internal frequencies into three externals of kilohertz. The 500 MHz frequency perfectly matches with the predicted result in 1% of variation. We could not test the 250 MHz signal. Thus, we omitted it in the picture. Another pin pad assignment is being investigated to solve this problem.

The 750 MHz test exceeded predictions, measuring approximately 120 kHz, a difference of 25%. This measurement suggests an internal clock of 1 GHz, which is desirable but not implemented. Figure 5. illustrates the signals testing.

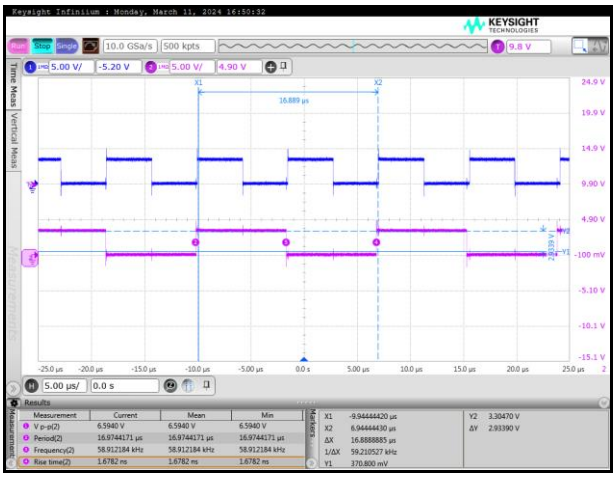

Fig.5. *Oscilloscope measure of 60 and unpredicted 120 kHz.*

Additional tests and studies will be conducted to comprehend this result. Performing some settings, an internal clock family is viable for high-range and high-resolution in TDC applications.

4. Conclusions and Future Works

Three internal high-frequency FPGA oscillators were designed, simulated, and tested using a fast-prototyping low-cost DE10-Nano development board. The 500MHz clock matched with predicted design. A review of some inconsistencies found at 250 and 750 MHz must be conducted. After solving this, the number of family members will increase, focusing on resolution and range. Designing internal frequencies upper 1Ghz is in development.

After the characterization of these digital oscillators, the techniques of high-resolution TDC will be gradually implemented as multi-phased clocks and pulse-shrinking TDC. In conclusion, an internal clock family is viable for high-range and high-resolution TDC applications.

Acknowledgements

The authors express their acknowledgement to their respective institutions and the National Council for Scientific and Technological Development (CNPq) under the CPSAE Project (Grant No. 422360/2023-6) for supporting the development of this work.

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Threshold voltage rebound effect on MISHEMT devices

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1. Abstract

In this work, the threshold voltage rebound effect and a similar kink effect were studied for a MISHEMT operating in temperatures ranging from 200 K up to 450 K. In the transfer curve, is possible to see a ZTC region forming for increasing temperature from 200 K up to 325 K, however for temperatures over 350 K the threshold voltage behaves in the opposite direction, giving birth to a threshold voltage rebound effect. In the output characteristic, for increasing overdrive voltage, is possible to see a shift of like kink effect toward to higher drain voltages.

2. Introduction

Despite the good performance and resilience to harsh environments exhibited by the High Electron Mobility Transistor (HEMT) [1], its progress is hampered by challenges such as increased gate leakage current and drain current collapse. To address these limitations, an insulator between the gate and the semiconductor is introduced, giving birth to the Metal-Insulator-Semiconductor High Electron Mobility Transistor (MISHEMT) [2-4]. Recent studies have identified multiple conduction mechanisms at different interfaces within the MISHEMT, encompassing both HEMT and MOS conductions [5, 6]. This work studies the rebound effect of the threshold voltage of a MISHEMT operating under different temperatures, and the kink effect that happens for high overdrive voltages.

3. Device characteristics

The device studied in this work is a MISHEMT with gate length of 600 nm and width of 5 µm, an Si_3N_4 insulator of 2 nm, an AlGaN barrier layer of 15 nm, an AlN spacer of 1 nm, and a GaN buffer layer of 2.5 µm operating in temperatures ranging from 200 K to 450 K. The device was fabricated at imec – Belgium. – and more details can be found in [3].

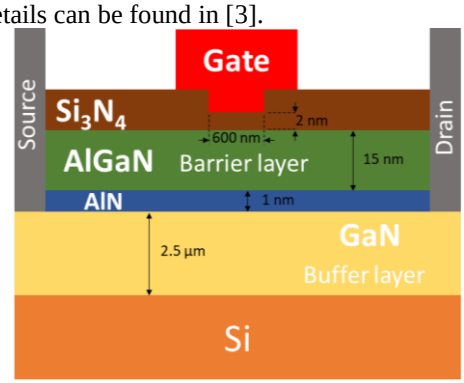

Fig.1. *Schematic cross section of a MISHEMT.*

4. Results and analysis

Figure 2 presents the drain current (I_{DS}) X gate voltage (V_{GS}) for multiple temperatures. From 200K to 350 is possible to see a shift of the threshold voltage (V_{TH}) to the left and a decrease in current level due to mobility degradation, giving birth to a ZTC region. However, for temperatures 350 K and above, a rebound effect shifts the V_{TH} to the right. This effect is better observed through the V_{TH} as a function of temperature presented in figure 3.

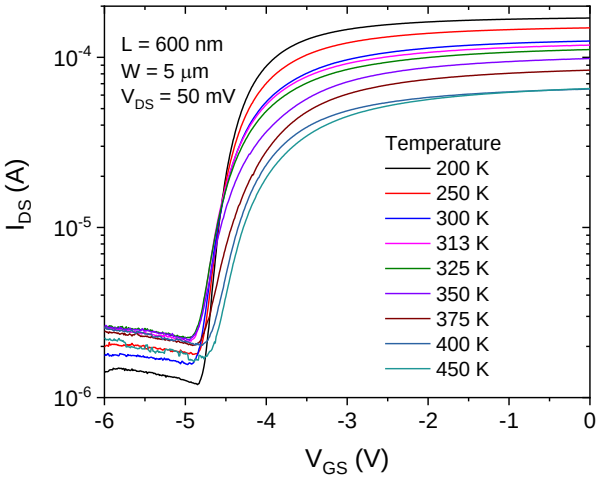

Fig.2. *Drain current as a function of gate voltage for multiple temperatures for a MISHEMT with gate length of 600 nm.*

For increasing temperature, the V_{TH} decreases until 350 K due to depletion depth reduction which affects the MOS conduction present in the device. Although, for temperatures above 350 K a rebound effect kicks in and increases the V_{TH}, possibly increasing the number of traps and altering the trap energy in traps presents in the AlGaN/AlN and AlN/GaN interfaces. In turn, the ionized traps capture more electron, reducing the positive charges in the interfaces and shifting the V_{TH} to the right. This affects mostly the HEMT conduction.

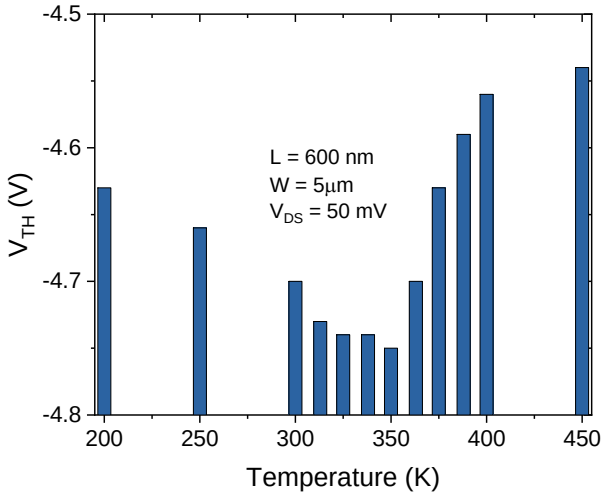

Fig.3. *Threshold voltage as a function of temperature.*

In figure 4 the drain current as a function of drain voltage for multiple VGT is presented. For low VGT, the MISHEMT behaves as expected presenter a clear linear and saturation region, however, for higher VGTs there is an increase in the current for specific VDS biases, creating a sort of kink effect in the curve. This effect happens due to the different conduction mechanisms (HEMT and MOS). This effect will be called MISHEMT kink effect (MH kink effect).

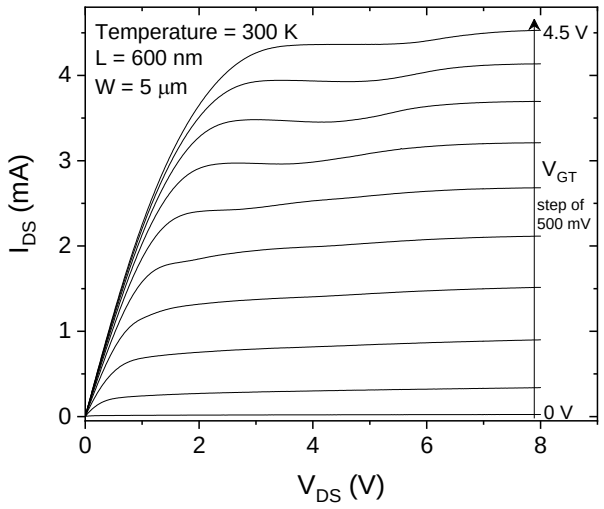

Fig.4. *Drain current as a function of drain voltage for V_{GT} ranging from 0 V to 4.5 V.*

The MH kink effect in figure 5 represents the V_{DS} which the anomaly happens, as a function of V_{GT}. It is possible to observer an increasing MH kink for increasing VGT, thus reaching a point where the curve changes its ratio and presenting a reduction in the increase. This behavior is most likely due to a saturation of the number of carriers in the 2DEG.

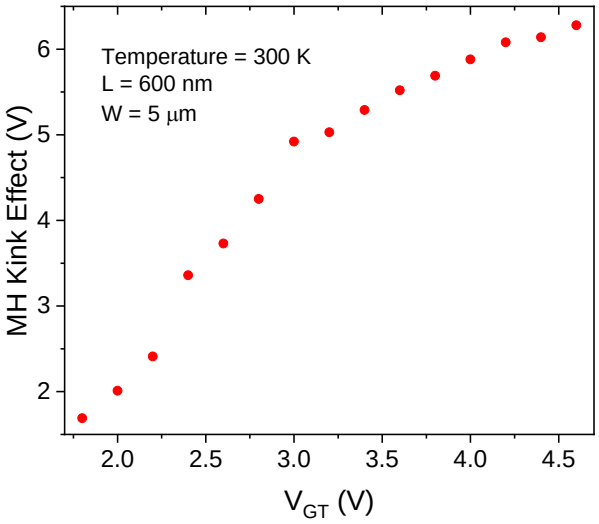

Fig.5. *MH kink effect as a function of V_{GT}.*

5. Conclusions

The threshold voltage rebound effect and the MH kink effect were studied in this work. The device presented a rebound effect when operating under different temperatures due to the competition of effects present in the MOS and HEMT conductions. A kink effect when operating under multiple V_{GT} bias conditions was observed because the MOS conduction saturates first than the HEMT one, creating the anomaly.

Acknowledgments

The authors would like to thank CAPES and CNPq for the financial support and Imec for providing the samples used in this work.

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Microfabrication of Diffractive Grating by Direct Laser Writing using Hermitian Spectrum

1. Abstract

A diffractive grating microrelief is capable of modulating the phase of an incoming wavefront light using diffraction to generate optical patterns. Limiting the phase variation within 0 – π interval, the Hermitian spectrum occurs, with real and complex conjugate values. This study aims to explore these properties in the fabrication of microrelief.

2. Introduction

Diffraction of light occurs when it encounters an obstacle close to its wavelength, forming specific patterns. The scalar theory of diffraction, proposed by Huygens and Fresnel, describes the propagation of light through secondary waves, revealing its vectorial nature [1]. In turn, digital holography, developed by A. Lohmann and others, uses algorithms such as iterative Fourier Transform Algorihtm (IFTA) to reconstruct wavefront data, providing good results [2].

The IFTA method uses an image and its Fourier transform to obtain the diffraction spectrum, to be encoded by the hologram medium in order to modulate an incoming wavefront. Binary phase modulation results in a conjugate complex optical distribution due to the real-valued distribution of the hologram, characterising it as a Hermitian spectrum. Binary optics technique can be employed to fabricate the device using processes similar to those of integrated circuits and MEMS [3].

3. Methods

A. Diffractive Array Design

The IFTA method uses a digital image (Fig. 1(a)) and applies the FFT in the reverse direction of light, following the theory of scalar diffraction to describe the distribution of the harmonic Fourier function,

$$G_{x'y'} = FT(f_{xy}) = |f_{x'y'}| \exp[i\,\phi_G(x'y')] \qquad (1)$$

$G_{x'y'}$ is the distribution of diffracted points, with coordinates (x'y'), while FT represents the Fourier transform operator, implemented by the Fast Fourier Transform (FFT) algorithm. The amplitude $|f_{x'y'}|$and the phase φ_G(x'y') describe the complex function in spatial frequency space [4].

The result allows extracting the diffractive grating plane with phase and amplitude. By constricting the phase modulation distribution to two values (0 and π), the inverse FT shows the propagation of light from the hologram to the diffraction pattern, resulting in a real-valued two - dimensional distribution in the reconstruction plane ($g^*_{xy} = |g^*_{xy}|\exp[i\phi_{xy}]$) [4].

When applying the described behaviour, a conjugate complex image emerges due to the distribution of the hologram consisting only of real values, following the Hermitian spectrum ([f g] = [g f]*). The hermiticity of a square matrix A is verified by equality with its conjugate transpose, as illustrated in Fig. 1(b) [5].

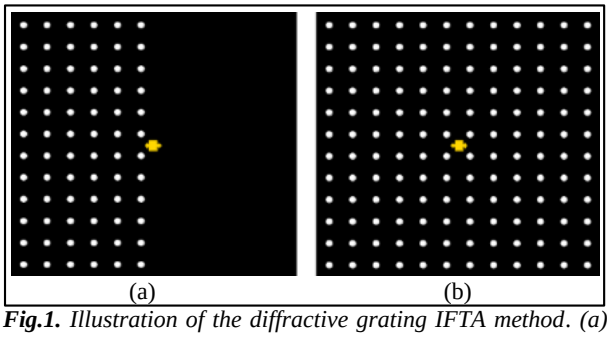

Fig.1. *Illustration of the diffractive grating IFTA method. (a) Initial image (Matrix A – 6 x 12 points). (b) Corresponding Hermitian Distribution (Matrix A*) - 12 x 12 points.*

B. Fabrication of the diffractive grating

The device was fabricated using photoresist deposited on top of a glass substrate, following specific steps: 1) Cleaning the glass substrate: The sample was cleaned using a cleaning cycle with trichloroethylene, acetone and isopropanol at 80 °C for 10 minutes, followed by drying with N_2 flow; then, the slide was dehydrated at 120 ºC for 15 minutes. 2) Preparation and deposition of the resist: Application adhesion promoter at 5000 rpm for 30 seconds, followed by evaporation of the solvent at 120 ºC for 70 seconds; resist coating (AZ-5214) at 4000 rpm for 30 seconds, followed by preheating at 90 ºC for 5 minutes, resulting in a resist thickness of 4 µm. 3) Lithography: Direct laser writing at 180 mJ/cm² (2 µm resolution); development with MIF 300 : H_2O-DI for 40 seconds. 4) In order to tune the phase grating, O_2 plasma etching was used with a power of 150 W, pressure of 100 mTorr and oxigen flow of 50 sccm. The etching rate was 0.04 µm/min for 30 minutes, resulting in a remained resist thickness of 2.8 µm. Fig. 2 shows the process steps to fabricate the diffraction grating using the IFTA hologram.

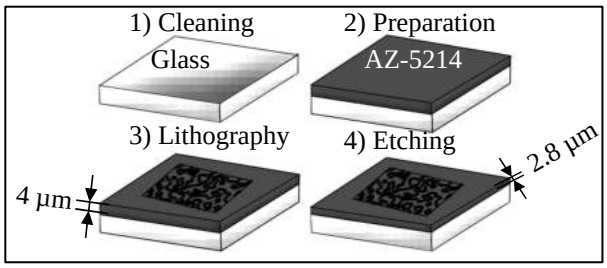

Fig.2. *Schematic view of the process steps, as well as the methodology used to fabrication the diffraction grating.*

The thin surface profile is implemented by generating a variation of the thickness $d_G(f_x f_y)$, by using the following relation

$$d_G(f_x f_y) = \frac{\lambda}{2\pi(n_R - 1)} \phi_G(f_x f_y) * N \qquad (2)$$

where N is an odd integer, $d_G(f_x,f_y)$ is the thickness variation distribution along the grating surface, ϕ_G is the phase delay distribution along the grating surface, nR is the refractive index of the material the grating is implemented (resist in this case) and λ is the operating wavelength. Assuming, N = 5, n_R = 1.55, λ = 633 nm, and phase delay ϕ_G = π, the desired step height value is d_G = 5* {633 / [2(1.55 - 1)]} = 2870 nm.

3. Result and conclusion

Fig. 3(a) shows the distribution of binary complex values, obtained by the IFTA method. This image is the computational holographic "mask" used in direct writing. Fig. 3(b) shows the simulation of the diffractivion pattern generated by the binary phase-only of Fig. 3(a).

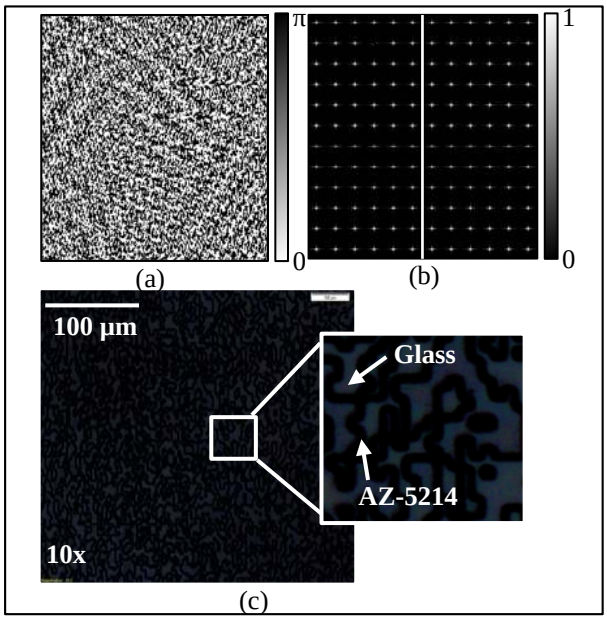

Fig.3. *(a) Holographic distribution generated by the IFTA method (256 x 256 pixels). (b) Fraunhofer diffraction pattern (Matrix A and conjugated Hermitine Matrix A*). (c) Optical microscopy of the fabricated microrelief.*

The schematic arrangement for obtaining the diffractive pattern is outlined in Fig. 4(a). Briefly, a laser light source is directed at the optical device, resulting in the generation of a diffractive pattern. The images were acquired using a cell phone camera positioned at a distance of 1 cm from the laser light source. Therefore, the optical characterization of the produced device is presented in Fig. 4(b).

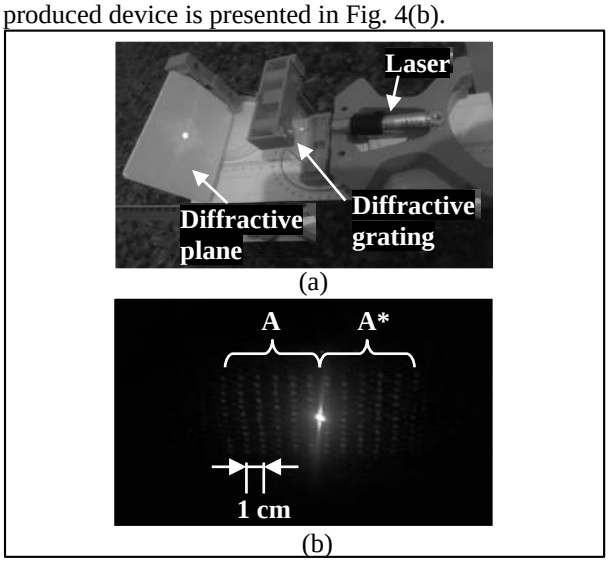

Fig.4. *Optical characterization of the diffractive grating. (a) Experimental apparatus. (b) Generated diffractive pattern. Where A is the reconstruction of the real image and A* is the Hermitian distribution of the real image.*

The results obtained in the simulation corroborate studies in the literature [2 - 4]. Furthermore, the optical behavior observed in the characterization of Fig. 4(b) has a diffraction pattern similar to the simulation in Fig. 3(b), validating this study. Therefore, a matrix of 6 x 12 points can generate 12 x 12 points using the Hermite spectrum in the Fourier transform.

Acknowledgments

This study was financed in part by the Coordenação de Aperfeiçoamento de Pessoal de Nível Superior – Brasil (CAPES - PROEXC) – Finance Code - 88887.673229/2022-00. The support of the facilities of the Center for Semiconductor Components and Nanotechnology (CCSNano) and Renato Archer Information Technology Center – CTI.

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Fabrication and characterization of highly strained silicon nanowires for sensing applications

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1. Abstract

In this work, we aim to fabricate strained silicon nanowires (sSiNWs) to study electric mobility and giant piezoresistance. Through techniques compatible with the CMOS technology, individual NWs were fabricated from strained silicon-on-insulator (sSOI) thin films with 0.8% biaxial strain. Subsequently, the buried oxide (BOX) is removed from the SOI film, thus suspending the NWs, and the new boundary condition of its surface induces a mechanical stress amplification, now uniaxial in the NW longitudinal direction. The proposal is to stress the NWs to levels higher than those employed in industry. Parameter optimization can further result in the fabrication of MOSFETs based on ultra-strained NW in *Gate All Around* (GAA) topology, and chemical and physical sensors for various technological applications.

2. Introduction

The industry has employed the mechanical straining of the active region of transistors since around 2004 as a way to improve the device's performance. Mechanical stress increases the carrier mobility and allows for higher clock frequencies of logic circuits, as well as overall processor performance [1]. Recent studies show that mechanical stress can change semiconductor band structure and, hence, the charge distribution on the NW surface [2], which can be beneficial for applications in chemical and physical sensors.

sSiNWs can exhibit giant piezoresistance effect [3], which consists of the modulation of the material electrical resistivity under the influence of mechanical stress. Several studies have been carried out with theoretical explanations and different approaches. However, works with sSiNW with higher deformations (> 2%) are scarce, especially without external actuators for driving stress.

In this sense, this work demonstrates that sSiNWs can be fabricated in a CMOS-compatible platform and further strained at relatively high levels without external actuators, which is interesting from the technological point of view. The devices offer a huge potential in applications of highly sensitive pressure and force sensors, as well as in the fabrication of high-performance microelectronics with sensitivity to physical and chemical stimuli.

3. Methodology

A. Strained Silicon on Insulator (sSOI)

The sSOI substrate consists of an undoped 15 nm-thick silicon film with 0.8% biaxial strain (about 1.44 GPa of biaxial stress in the [110] and [-110] directions). The silicon film relies on the top of a 145 nm-thick buried silicon dioxide on a bulk silicon substrate. The crystallographic orientation of the silicon surface is (001).

B. Device Fabrication

Initially, we spin-coat the electrosensitive resist PMMA ARP 679.04 at 4000 rpm for 30 seconds and evaporate the solvent on a hot plate at 180 ºC for 2 minutes. Then, we expose the resist using electron beam lithography system. The resist was developed with ARP 600.56 for 2 minutes. Afterward, the wafers undergo a dry etching process in an ICP-RIE plasma system, which is used to etch the Si and define the NW. Then, an organic cleaning protocol with acetone and isopropanol is performed to remove any remaining resist. Finally, in order to suspend the sSiNWs, we use a buffered hydrofluoric acid (BHF) solution for approximately 3 minutes to remove the silicon oxide underneath the sSiNWs.

4. Results and Discussions

A. Suspended Nanowires

The dimensions of the suspended nanowires, such as width and length, were controlled by the lithography parameters, thus leading to distinct residual stresses in the sSiNWs. In this sense, one can obtain different piezoresistance values by varying the sSiNW width and length. The length of the sSiNW varied from 0.5 to 2.5 µm, while its width ranged from 50 to 400 nm. Figure 1 shows an example of the fabricated suspended sSiNWs. Note that the pads are the peripheral region at the ends of the nanowires. The width of the pads also varied in this experiment between 0.5 to 1.75 µm, being wider than the width of the nanowires. The pads are partially or fully suspended, depending on their dimensions and the etching time in BHF. Simulations conducted by our group using the finite element method (FEM) in COMSOL show that before the removal of SiO_2, the nanowires exhibit predominantly uniaxial strain of around 0.8%, while the pads show a 0.8% biaxial strain. However, removing the SiO_2 underneath the nanowires and pads modifies the boundary conditions on the silicon surface, thus relaxing the pads, which amplifies the stress on the NWs [3]. The sSiNWs ultimately exhibit amplified uniaxial stress magnitude depending on their dimensions.

B. Raman characterization

Raman spectroscopy is a highly versatile

technique used in this work to track the residual mechanical stress in sSiNWs. For the unstrained silicon, the Raman peak position is $\omega_0 = 520.5$ cm^{-1}. On the other hand, in the strained silicon, the mechanical stress disturbs the vibrational modes of the crystal lattice and shifts the strained Raman peak (ω_i) to the left (in the case of tension) [4].

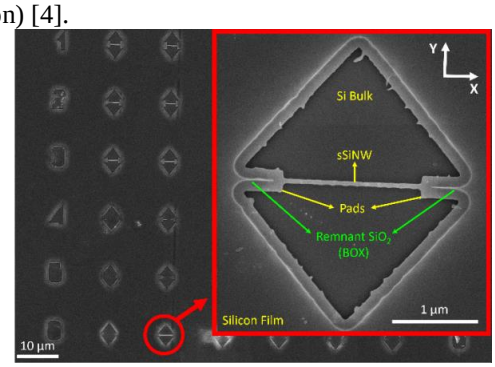

Fig. 1. *sSiNW with length and width of 2.5 µm and 90 nm, respectively.*

The Raman shift between unstrained and strained silicon, $\Delta\omega = \omega_i - \omega_0$, allows for indirectly obtaining the stress along the [110] crystallographic direction (σ_{xx}) of the sSiNW. As the thickness of the nanowire is at least one order of magnitude lower than the length and width, we can neglect the stress in the Z direction (σ_{ZZ}). Equation (1) characterizes the Raman shift [3] as a function of the in-plane stress:

$$\Delta\omega = \frac{1}{2\omega 0}\{[pS_{12} + q(S_{11} + S_{12})] \times (\sigma_{XX} + \sigma_{YY})\}$$
$$= \mathbf{SSC} \times (\sigma_{XX} + \sigma_{YY}) \quad (1)$$

$\Delta\omega$ is the Raman shift, p and q are the phonon deformation potentials (PDPs) of silicon, and S_{11} and S_{12} are the silicon's elastic constants (Pa^{-1}) obtained from the compliance matrix. σ_{YY} and σ_{ZZ} are stresses in the crystallographic directions [-110] and [001]. Here, the Stress Shift Coefficient (SSC), in units of $cm^{-1}Pa^{-1}$, linearly relates stresses and Raman shift of a tensile sample and depends on the PDPs (p and q) and their elastic constants (S_{11} and S_{12}). Spejo et al. [3] reports that the **SSC** is around $-1.9 \pm 0.1 \times 10^{-9}\ cm^{-1}Pa^{-1}$.

Figure 2 shows a Raman spectrum of a 300 nm wide sSiNW showing the peaks of bulk Si (unstrained) and sSiNW. It is worth mentioning that the diameter of the laser beam is larger than the width of the nanowires. Therefore, both the bulk Si peak at ω_0 = 520.5 cm^{-1} and the sSiNW peak were detected concurrently in the Raman spectrum. In our measurements, the stress in the Y direction cannot yet be neglected, as the width of the nanowires presented here does not guarantee predominantly uniaxial stress. For sSiNWs of different widths, similar $\Delta\omega$ values were obtained. For 750 nm, 300 nm, and 200 nm-wide sSiNWs, $\Delta\omega$ values of -4.36 cm^{-1}, -4.59 cm^{-1} and -5.55 cm^{-1}, respectively, were obtained. It should be mentioned that these results refer to sSiNWs whose pads were not completely suspended. Therefore, the sSiNWs were not ensured to be uniaxially strained and at the maximum stress. In fact, FEM simulation suggests that narrow nanowires with predominantly uniaxial stress should present larger $\Delta\omega$ values.

The $\Delta\omega$ of the 750 nm and 300 nm wide sSiNWs are comparable, thus suggesting residual stress in the Y direction. As shown in Eq. (1), the Y component contributes to the increase in $\Delta\omega$, thus causing the 750 nm wide biaxially strained sSiNW to have a higher $\Delta\omega$ value compared to the narrow nanowire. On the other hand, comparing the $\Delta\omega$ value for 300 nm and 200 nm wide sSiNWs, the shape anisotropy of such narrow nanowires leads to a reduction of the σ_{YY} component. Hence, they become predominantly uniaxially stressed. Therefore, in this case, with a reduction of about 100 nm in the sSiNW width, it was already possible to observe an increase of about 1 cm^{-1} in $\Delta\omega$ due to an increase in the uniaxial stress (longitudinal direction) of the sSiNW. Hence, the increase in the σ_{XX} component yields an increase in $\Delta\omega$, as expected.

Therefore, considering that the 200 nm wide sSiNW already has predominantly uniaxial stress, we can neglect σ_{YY} in Eq. (1) and obtain the direct relationship between $\Delta\omega$ and σ_{XX}. In this case, the uniaxial stress obtained was 2.87 GPa, which is higher than that used in the industry, limited to about 1 GPa.

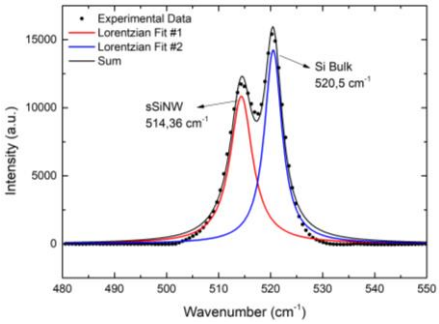

Fig.2. *The Raman peak for sSiNW was observed at 514.36 cm^{-1}. We used the Horiba XploRA with a 532 nm laser for the measurements.*

5. Conclusions

Strained silicon nanowires were fabricated using techniques compatible with the CMOS technology. The mechanical stress was achieved without external actuators. Raman spectroscopy was used to characterize the mechanical stresses of around 2.87 GPa (uniaxial) for 200 nm-wide sSiNWs. The next stage of this work involves measuring the giant piezoresistance for stress larger than 4 GPa, which requires process parameter improvements.

Acknowledgments

The authors thank CCSNano/UNICAMP. This work was financially supported by FAPESP (2022/16809-2) and CNPq (310021/2021-9 and 406193/2022-3)

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Mach Zehnder Interferometers in Photonic Circuits for Solar Irradiance Investigations

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1. Abstract

The Sun's influence on Earth's climate through Total Solar Irradiance (TSI) has sparked significant interest in understanding solar activity's long-term effects. This paper delves into the development of a prototype Mach-Zehnder Interferometer-based radiometer sensor for temperature detection. Fabrication processes involving pedestal-style waveguides were conducted, and preliminary results indicate promising feasibility. Scanning electron microscopy (SEM) images demonstrate the integrity and uniformity of the waveguide structures. These findings lay a solid foundation for further exploration and potential applications in photonic devices.

2. Introduction

The Sun holds paramount influence over humanity. Its visible surface, the photosphere, emits radiant energy and hosts phenomena like sunspots, faculae, and granulation. This solar energy significantly impacts Earth's climate, primarily through Total Solar Irradiance (TSI), which powers our climate systems. The link between long-term temperature variations and solar activity has heightened interest in understanding the Sun's influence on Earth's climate [1], [2].

Understanding Total Solar Irradiance (TSI) demands rigorous accuracy, cadence, and stability in radiometers. Despite continuous spaceborne irradiance measurements since 1978, challenges persist. Electrical Substitution Radiometers (ESR) are the primary instruments for comparing absorbed radiant power with electric heating. Although ESRs have advanced, limitations such as prolonged thermal equilibrium durations and high thermal noise levels persist. To surmount these challenges, researchers explore alternatives like thermo-optic sensors [3], [4].

Current research in thermo-optic devices leverages the thermo-optic effect of materials, where temperature fluctuations alter refractive indices, influencing optical properties. Devices like the Mach-Zehnder Interferometer (MZI) exploit this effect through optical interferometry [5].

The MZI, harnessing total internal reflection, evenly splits light intensity between its arms. In an ideal setup, input and output light intensities equalize due to constructive interference. The thermo-optic effect, resulting from refractive index variations with temperature, leads to phase differences between interferometer arms. Consequently, non-constructive interference alters light output intensity, facilitating parameter analysis such as temperature or electric current detection[6].

Here are the preliminary results of a prototype investigating the feasibility of using a single-substrate Mach-Zehnder interferometer for temperature detection in a radiometer sensor.

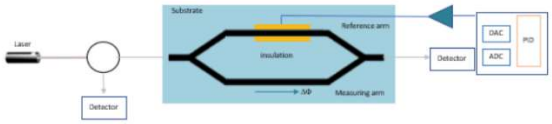

Fig.1. *Mach-Zehnder Interferometer-based radiometer sensor idea*

3. Materials and Methods

Fabrication of waveguides occurred at the Microelectronics Laboratory of the Department of Electronic Systems Engineering, University of São Paulo (USP). The manufacturing process involved several steps on P-type silicon wafers with (100) crystallographic orientation. Fig. 2 shows the fabrication process. Steps included (a) silicon wafer cleaning, (b) dry thermal oxidation, (c-d) photolithography, (e) wet oxide etching, (f) dry silicon etching, (g) a second cleaning process, (h) wet thermal oxidation and (i) the core layer deposition.

After initiating a chemical cleaning process to prevent contamination, the silicon substrate undergoes oxidation to form a silicon dioxide (SiO2) layer. Photolithography post-cleaning creates patterns using photoresist. Subsequent wet oxide etching and SF_6 dry silicon etching form the pedestal structure. A secondary cleaning readies the wafer for wet thermal oxidation, where SiO_2 reacts with silicon, forming a uniform silicon dioxide layer. These processes prepare the pedestal structure for waveguide core material deposition, completed through tantalum pentoxide (Ta_2O_5) sputtering.

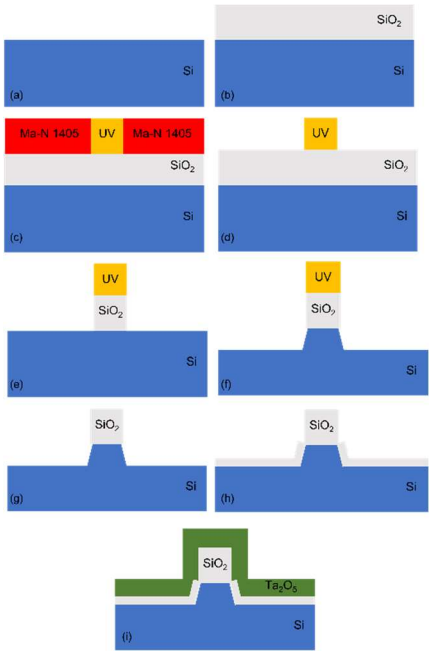

Fig.2. *Representation of the front section of the structure on the Si blade during the manufacturing steps of the pedestal structure.*

4. Preliminary Results

This study presents the preliminary results of manufacturing a Mach-Zehnder device using pedestal-style waveguides. The detailed manufacturing process was described in the previous section, where specific parameters were used for production, including a curvature radius R =32000 µm and a distance between arms D=100 µm. The waveguide thickness was kept constant at one µm. Analyses were performed using a scanning electron microscope (SEM) to assess the quality and precision of the manufactured device. Fig. 3 shows the images.

The images reveal details of the structure of the manufactured Mach-Zehnder device, highlighting essential aspects of the integrity and uniformity of the pedestal-style waveguides. Further analysis is underway to quantify specific parameters such as insertion losses and coupling efficiency.

5. Conclusions

In conclusion, this study explores the development of a prototype Mach-Zehnder Interferometer-based radiometer sensor for temperature detection, aiming to enhance understanding of the Sun's influence on Earth's climate. These preliminary results indicate the promising feasibility of manufacturing the Mach-Zehnder device using monomodal pedestal-style waveguides, providing a solid foundation for further investigations and potential applications in photonic devices.

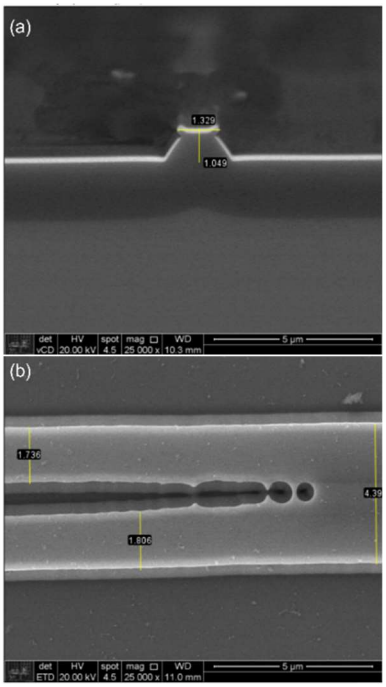

Fig.3. *SEM images from the pedestal structure (a) Cross-section and (b)top view of the Y detail*

Acknowledgments

The authors would like to thank CAPES, CNPq and FAPESP (grant 2023/01324-6) for the financial support during the execution of this work.

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Temperature influence in the current mirror designed with gate-all-around nanosheet MOSFETs

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1. Abstract

The focus of this work is the analyses of nanosheet gate-all-around transistors working as a current mirror in a range of temperature from -100 ºC up to 125ºC. The nanosheet transistors was modeled using the Look Up Table method and a Verilog-A language, based on experimental measurements. A current mirror circuit was designed and analyzed at different bias points based on the ZTC region. When biasing the circuit before ZTC point, the compliance voltage is higher, which means that the circuit reproduces a largest range of current indicating a larger saturation region. There is a influence of the temperature in the drain current level, but it did not cause a significant effect at the current mirror operation.

2. Introduction

Gate-all-around nanosheet field effect transistors (GAA-NSFETs) have emerged as a leading alternative for supplying the requirements for sub 5 nm technology nodes. These transistors supply the industry demand, providing faster circuits, an improved performance, and a lower power consumption. These improvements in the transistors are provided by the higher electrostatic coupling between gate and channel, due to gate-all-around structure, which also enables a reduction in the parasitic effects, such as, the short channel effect (SCE).

The temperature influence on the GAA-NS devices is very important since its application in integrated circuits with a very large integration density, reaches temperatures around 100 ◦C, and its applications at military or space application, achieves low temperatures. Since the current mirror is an essential building blocks for biasing integrated circuits, the analysis at harsh environments is very essential [1].

3. Experimental Details and Simulations

The analyzed device for this work is the n-type GAA vertically stacked NSFETs, that consists of 22 parallel fins in the device layout, with two vertically stacked silicon nanosheets. Each transistor has the following characteristics: channel width (W_{NS}) about 15 nm, channel height (h_{NS}) about 11 nm, effective oxide thickness (EOT) about 0.9 nm and the channel length (L_{gate}) of 100 nm. The effective-work function (EWF) metal in the gate stack results from a combination of TiN /Al-based material layer depositions with a total thickness of 7.5 nm. Fig. 1 A and B presents the Transmission Electron Microscopy (TEM) cross section images of the device, and the schematic cross section, respectively.

To develop the work, it was necessary the experimental measurements of the nanosheet transistors to create Lookup Tables (LUT), to enable the device modeling using the Verilog-A analog hardware description language. For model validation, the Virtuoso software from Cadence was used.

NMOS and PMOS nanosheet transistors were measured with a gate voltage (V_{GS}) from -0.5 V to 1.0 V, with a step of 10 mV, and a drain voltage (V_{DS}) from 0 V to 1.0 V, with a step of 10 mV. The temperatures analyzed were: -100°C, -40°C, 25°C, and 125°C.

Fig. 2 shows the transfer curve of NMOS (right) and PMOS (left) transistors, where open symbols correspond to experimental data, and closed symbols correspond to simulated data. Satisfactory modeling is observed for all analyzed temperatures, as the model data matched the experimental data.

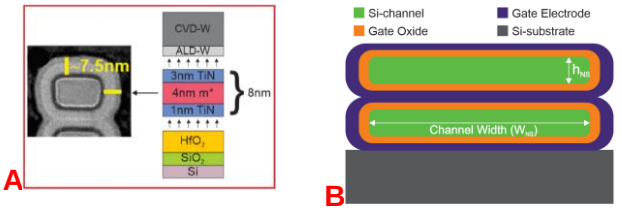

Fig. 1 *– A) Transmission Electron Microscopy (TEM) cross section images. B) Schematic cross section of a stacked nanosheet transistor [2].*

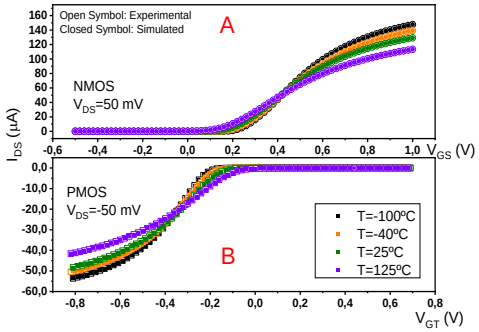

Fig. 2 *– Transfer curve for validating the NMOS (A) and PMOS (B) nanosheet transistor model.*

The Fig. 3 presents the analyzed current mirror [3]. The selection of this circuit for the reference current source was based on its simplicity and in the main design criterion is the same voltage drop (V_{DS}) across each of the transistors in series, $V_{DS} = V_{DD}/3$ in M1, MBiasP, and MBiasN, ensuring the same biasing condition for these devices for the same current value.

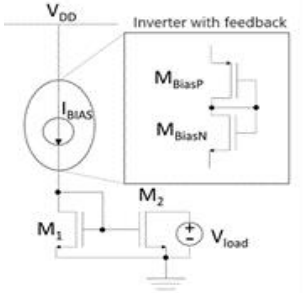

Fig. 3 *– N-type current mirror circuit, using the inverter with feedback as a source of bias current.*

The temperature influences the transistor behavior, as observed in Fig. 4, where the presence of a region unaffected by temperature, the Zero-Temperature- Coefficient (ZTC) region, can also be noted. Therefore, when defining a circuit biasing point, it is important to consider this region, since it is not desirable a temperature influence in the circuit behavior.

To analyze the temperature influence in the current mirror, three biasing points were chosen: the first before the ZTC region (V_{DD}=0.96V and V_D=0.32V), the second near the ZTC region (V_{DD}=1.16 V and V_D=0.39 V), and the third after the ZTC region (V_{DD}=2.52 V and V_D=0.84V).

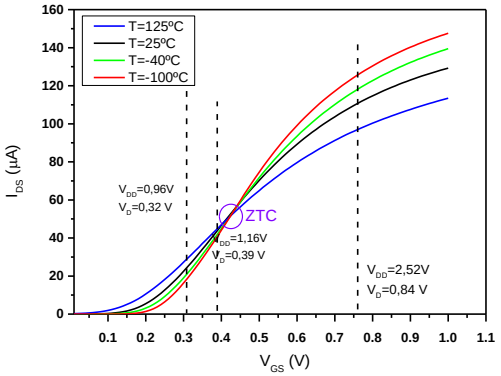

Fig. 4 *– IDS X VGS of nMOS, with polarization points chosen in relation to the ZTC point.*

Fig. 5 presents the drain current (left) and the output-over-input current ratio (relative output current) (right axis) of the current mirror biased before the ZTC region, both as functions of the load voltage (V_{load}). At this point, it is observed that increasing the temperature leads to an increase in the drain current, showing a variation of approximately 130 µA from -100 ºC to 125 ºC. This increase occurs because below the ZTC region, the predominant factor affecting the drain current with temperature is the threshold voltage [4]. Analyzing the relative output current, it is observed that it remains close to the ideal (represented by the dashed gray curve, with a value of 1) for a wide range of V_{load} (after saturation).

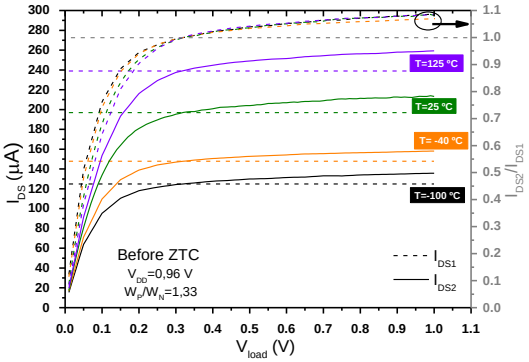

Fig. 5 *– Drain current (left) and I_{DS2}/I_{DS1} (right) as a function of V_{load} with the current mirror biased before the ZTC region.*

In Fig. 6 is presented the current mirror response for the bias point near to the ZTC region. As it is biased is near the ZTC region (a temperature-invariant region), a smaller variation in the drain current is observed when compared to the point before ZTC; in this case, the variation is approximately 80 µA (from -100 ºC to 125 ºC), where increasing the temperature leads to an increase in the drain current. The relative output current exhibits a behavior quite similar to the previous point, remaining close to the ideal for a wide range of V_{load}.

In Fig. 7, the circuit is biased at the point after ZTC. In this case, it is observed that increasing the temperature leads to a reduction in the drain current, since the predominant factor influencing the temperature is the mobility degradation [5]. From -100 ºC to 125 ºC, there is a reduction of 730 µA. The relative output current shows a narrower range of conformity with the ideal, indicating a shorter saturation range.

The compliance voltage is a key parameter in current mirror analysis, it determines how much the current I_{DS2} mirrors the current I_{DS1}, with up to a 10% margin of error [3]. Fig. 8 illustrates this voltage in relation to the gate voltage of transistor M2. The optimal scenario arises with the lowest biasing, where the compliance voltage varies from 0.80 V to 0.84 V as temperature decreases. This optimal compliance voltage is achieved by biasing the current mirror before the ZTC region.

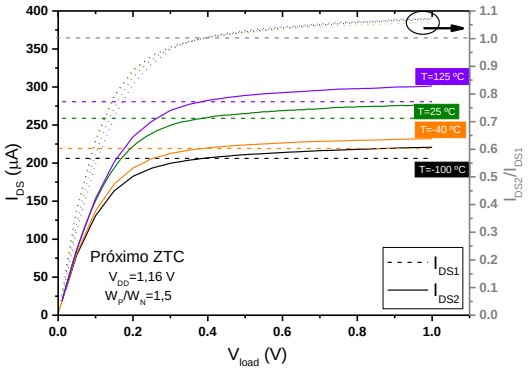

Fig. 6 *– Drain current (left) and I_{DS2}/I_{DS1} (right) as a function of V_{load} with the current mirror biased near the ZTC region.*

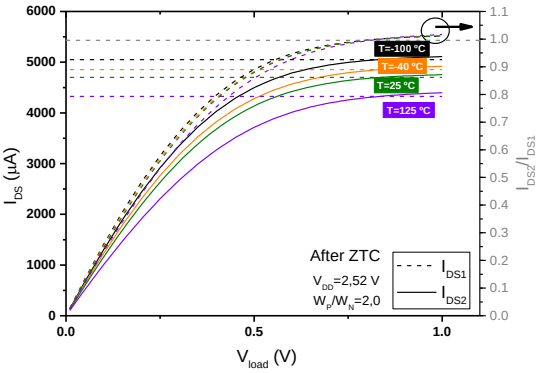

Fig. 7 *– Drain current (left) and I_{DS2}/I_{DS1} (right) as a function of V_{load} with the current mirror biased after the ZTC region.*

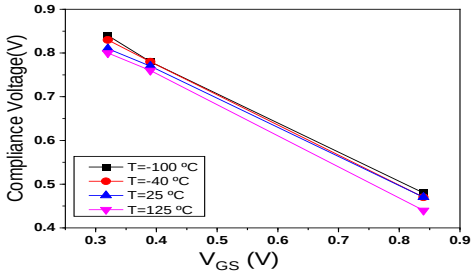

Fig. 8 *– Compliance voltage as a function of transistor M2 gate voltage.*

4. Conclusions

The nanosheet transistors were modeled in this work focusing on its application as current mirror. The current source was based on inverter with feedback (designed with the nanosheets). The temperature influence was analyzed in the current mirror circuit, in three regions, after, before and near the ZTC region. The current mirror presented a better behavior when biased at the points before and near the ZTC, presenting a larger range of mirroring, and a higher compliance voltage.

Acknowledgments

The authors would like to thank the imec for supply the devices and CNPq and CAPES for the financial support.

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Low-Temperature Effects on Mobility Degradation in Two-Level Stacked Nanowire MOSFETs

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1. Abstract

This study investigates carrier mobility and its degradation mechanisms concerning temperature variations in two-level stacked nanowire MOSFETs within the range of 100 K to 400 K. Results demonstrate that decreasing temperature enhances the peak transconductance value across all device geometries. Moreover, temperature reduction influences both the gate voltage at which the peak transconductance occurs and the peak low-field carrier mobility. An increase in the gate voltage required to achieve these peak values is observed with decreasing temperature. Additionally, the first-order degradation factor diminishes as temperature rises, while the second-order factor increases within the same temperature range.

2. Introduction

The Multiple-gate field-effect transistors (MuGFETs) have emerged as dependable devices, facilitating the continued downscaling of MOSFETs into the nanometer range[1], [2]. Among these, vertically stacked nanowire MOSFETs, also known as stacked nanowires, hold promise for future technological nodes [3], [4]. These devices effectively enhance the current density of nanometer-long MOSFETs without increasing the silicon footprint while maintaining commendable performance and scalability.

CMOS technology pervades everyday life to cutting-edge applications, operating under diverse temperature conditions. Understanding how fundamental parameters such as low-field carrier mobility and its degradation factors behave with temperature variation is of great importance for the design of reliable circuits and systems [5].

3. Results and Discussion

In Figure 1 and Figure 2, the I_D x V_G curves and the g_m x V_G curves are presented for the device with L = 100 nm W = 10 nm at temperatures ranging from 100K to 380K. From those curves, is noticeable the impact of temperature: a steeper slope in the subthreshold region and a higher transconductance value reached in a higher gate bias.

The data, show in Figure 3, delineates the temperature-dependent behavior of low-field carrier mobility across three discrete transistor widths: 10 nm, 20 nm, and 25 nm. Notably, a discernible trend emerges, indicating a more pronounced variation in low-field mobility with temperature for wider devices within the observed temperature range.

From Figure 4, a distinct pattern emerges as temperature increases, the first-order degradation factor θ_1 decreases, while the second-order degradation factor θ_2 increases. This trend holds consistently across all devices studied, regardless of channel width. A comparison of slope values from the tables reveals that θ_1 is more responsive to temperature fluctuations than θ_2, evident from the larger absolute slope values. Additionally, variations in these factors differ between FDSOI and planar CMOS technologies[6], [7], [8].

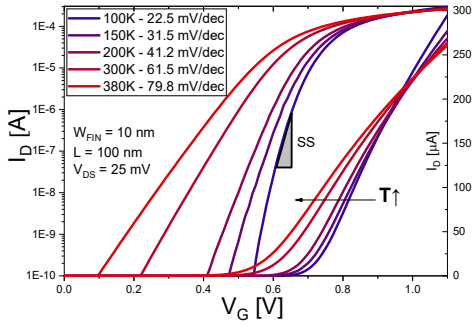

Figure 1 - Drain current as a function of gate bias with V_D= 25 mV. The same data is plotted in linear and logarithmic scales.

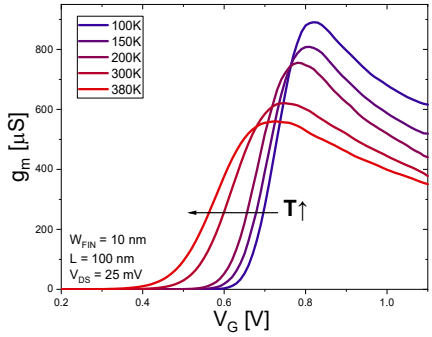

Figure 2 - Transconductance as a function of the gate bias.

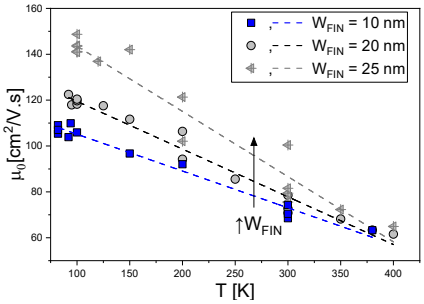

Figure 3 - Low-field mobility versus Temperature.

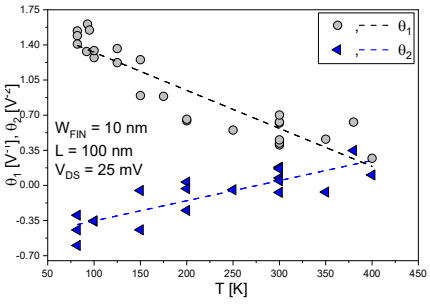

Figure 4 - Mobility degradation factors as a function of temperature for devices with W_{FIN} = 10nm.

4. Conclusions

In summary, this study offers a comprehensive analysis elucidating the intricate relationship between temperature, device characteristics, and performance metrics in 2-level stacked nanowire transistors with varying channel widths. Our analysis unveils temperature-dependent variations in threshold voltage, highlighting the emergence of the Zero-Temperature Coefficient (ZTC) around 0.95V. Notably, wider devices demonstrate heightened sensitivity to temperature fluctuations in low-field mobility, as evidenced by the data and supported by the presented slopes, underscoring the technology's robustness compared to alternatives. Furthermore, our examination of degradation factors reveals the nuanced impact of temperature on first-order (θ_1) and second-order (θ_2) degradation factors. We observe that θ_1 exhibits heightened sensitivity to temperature changes compared to θ_2, aligning with distinct scattering mechanisms dominated by surface roughness at lower temperatures.

Acknowledgments

This research was supported by the Coordenação de Aperfeiçoamento de Pessoal de Nivel Superior – Brazil (CAPES) under Finance Code 001, the National Council for Scientific and Technological Development (CNPq) (grant #140526/2023-4), and the Sao Paulo Research Foundation (FAPESP grant #2019/15500-5). Additional-ly, the paper acknowledges the support from the French Public Authorities through the NANO 2017 program. Furthermore, this work received partial funding from the SUPERAID7 project (grant Nº 688101).

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Investigation of AlGaN/GaN High-Electron Mobility Transistors

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1. Abstract

The performance of AlGaN/GaN-based High Electron Mobility Transistors (HEMTs) has been studied to assess the impact of varying gate lengths (L_g) on threshold voltage (V_T), transconductance (g_m), and subthreshold slope (S) output conductance (g_d) and series resistance (R_{SD}). The results indicate a better performance with the decrease of the channel length.

2. Introduction

AlGaN/GaN high electron mobility transistors (HEMTs) represent exceptional options for high-power, high-frequency, and high-temperature applications [1-2]. In RF power applications, these devices surpass previous alternatives, thanks to their wider band gap, elevated mobility, and dense electron population within the 2-dimensional electron gas (2DEG) region at the AlGaN/GaN interface [3-4]. The thermal and electrical characteristics of AlGaN/GaN or GaN devices are pivotal factors that impact their operational efficiency and reliability [1].

The integration of GaN devices into technology platforms is crucial for advancing power and RF applications. However, the current GaN technology, which relies on non-Si substrates, poses challenges due to its high cost and limited wafer size. Transitioning to a 200 mm Si complementary metal oxide semiconductor (CMOS) platform and adopting standardized fabrication tools are essential steps to facilitate the adoption of GaN devices for RF applications. These devices share similarities with n-channel MOSFETs (oxide-metal-semiconductor field-effect transistors) but are composed of multiple semiconductor layers rather than silicon. Furthermore, the drain current (Id) flowing between the source and drain terminals is regulated by the voltage applied between the gate and source terminals (V_g).

There's indeed a direct correlation between the length of the transistor channel (often represented as the channel width in HEMTs) and several crucial electrical characteristics, which are intricately linked to the device's design. Specifically, in HEMTs, the transconductance can be significantly impacted by the channel length. Typically, a higher transconductance is sought after as it directly translates to improved amplification performance.

Output conductance is related to the transistor's ability to supply current to the load circuit. It may be affected by the channel length, as it can influence the transistor's conduction characteristics. Threshold voltage is the Applied voltage required to initiate conduction in the transistor. Channel length can impact the threshold voltage and source and drain resistance is linked to the difficulty the current encounters while passing through the transistor. Channel length also can influence resistance, but other design factors, like doping profile and transistor geometry, also play a crucial role [5-6].

3. Device Studied

The studied HEMT (fig. 1) is composed of a high resistivity substrate of silicon <111>, with a 2 µm layer on the cap. The channel has a GaN layer with a thickness of 300nm, on top of an AlN spacer with a thickness of 1nm that helps in a good performance of density, mobility and drain current. The HEMT also has a 15nm barrier with Al 0.25 and Ga 0.75 where 0.25 is the mole fraction of aluminum and 0.75 is the mole fraction of gallium. A cover of SI_3N_4 and SiO as material thickness is added between 2DEG and gate metal More processing details can be found in [7].

At first, the characteristic curves of drain current and gate voltage (I_dxV_g with drain to source voltage (V_{DS}) of 4V and drain current versus drain and source voltage with V_g = 0.2V were analyzed at 25°C in different devices gate length (L_g) of 0.2, 0.4, 1µm and width (W) of 1 µm.

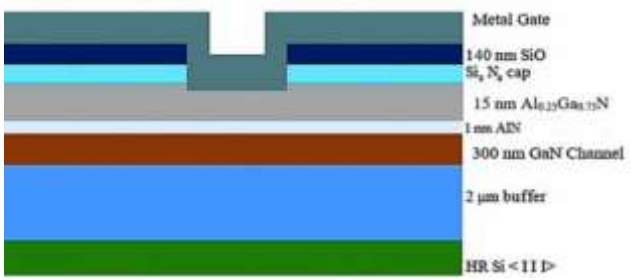

Fig.1. *Cross section of the transistor HEMT structure.*

4. Results and Discussion

Figures 2 and 3 illustrate significant trends in HEMTs with varying channel lengths. In Figure 2, it's apparent that the drain current (I_d) is notably higher in HEMTs featuring shorter channel lengths. This observation suggests that reducing the channel length enhances the transistor's ability to conduct current from the source to the drain.

Similarly, in Figure 3, the transconductance curves depict that the maximum current flowing along the channel is greater in HEMTs with shorter L_g. This indicates that decreasing the channel length leads to an increase in transconductance, highlighting the transistor's improved capability to amplify signals effectively. These findings underscore the importance of channel length optimization in HEMT design, as shorter channel lengths contribute to higher drain currents and enhanced transconductance, thereby improving the overall performance of the device.

Table I shows the behavior of V_T, g_d, g_m, R_SD, I_d, and the subthreshold slope (S). It is observed that as L_G decreases, we obtain: lower V_T; lower g_m specifically when the gate voltage V_g = 0.2 V (g_(m.max) increases if L_g is smaller, as shown in Figure 3); and R_SD will also be lower, thus allowing a greater g_D and greater I_D, which confirms Ohm's law. Studies conducted on different transistors with V_g > 0.2 V show that S decreases with increasing L_G. In this research, S remained constant, it is also known that with the increase of L_g, there will be a decrease in S. In other works, it is enough to verify with which value of L_g this change in S will be more or less significant for the behavior of HEMT's transistor.

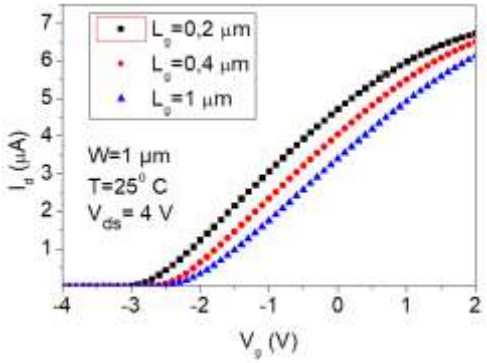

Fig.2. *$I_D x V_G$ curves for $V_{DS} = 4\ V$ with L_g variation.*

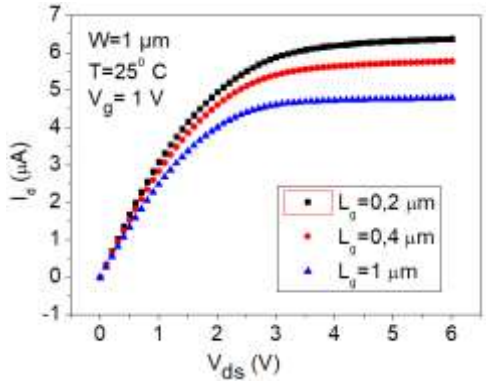

Fig.2. *$I_D x V_{ds}$ curves for $V_g = 1\ V$ with L_g variation.*

Table I. *Main parameters for mobility extraction*

L_g $10^{-6}m$	V_T V	g_d $10^{-4}S$	g_m $10^{-6}S$	R_{SD} $10^{3}\Omega$	I_d $10^{-6}A$	S mV/dec
0.2	-2.71	3.38	1.8	0,64	6.2	100
0.4	-2.32	3.06	1.7	0.69	5.8	100
1	-2.16	2.67	1.4	0,80	5.2	100

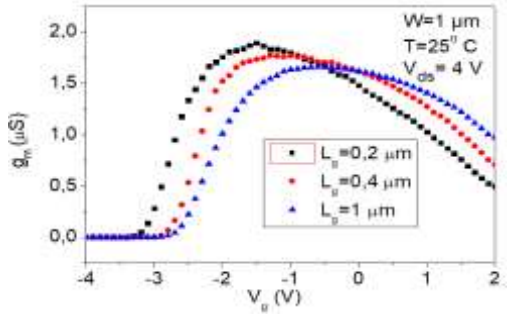

Fig.3. *$g_m x V_G$ curves with L_g variation.*

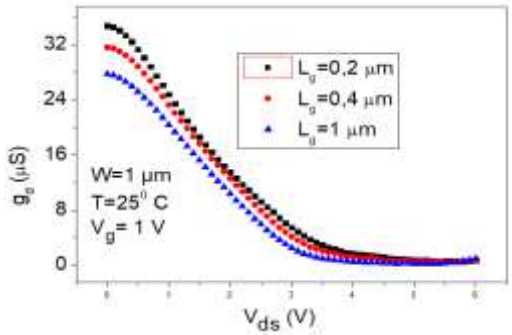

Fig.3. *$g_d x V_{ds}$ curves with L_g variation.*

5. Conclusions

This study revealed that an increase in channel length correlates with an increase in threshold voltage and drain and source resistance due to their direct relationship. However, an increase in channel length is inversely related to transconductance, output conductance, and drain current.

Acknowledgments

The authors thank imec ARF team in for having provided the samples studied and also to the Brazilian research-funding agency CAADI (Coordenadoria de Ações Afirmativas, Diversidade e Equidade) FAPESP (Process Nº: 2023/00123-7) and for supporting the development of this work.

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Operation of Ω-Gate SOI Nanowire MOSFETs down to 82 Kelvin

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1. Abstract

This work presents the electrical characterization of Ω-gate SOI nanowire MOSFETs in the temperature range from 82 K to 350 K. Devices with different fin widths are compared. The comparison is performed using experimental data looking for some of the fundamental electrical parameters such as threshold voltage, inverse subthreshold slope, and carrier mobility over the temperature.

2. Introduction

The exploration of MOSFET operation at low temperatures has sparked considerable interest owing to its potential for improving electronic device performance, such as minimizing the inverse subthreshold slope and addressing short-channel effects [1]. This temperature domain holds particular significance for applications in medicine and aerospace [2]. Furthermore, the burgeoning attention towards CryoCMOS for integration into quantum computing systems [3] serves as a compelling motivation for thorough low-temperature characterization efforts.

Therefore, this paper describes the operation of Ω-gate SOI nanowires in the temperature range of 82 K to 350 K. The fundamental device parameters, such as Threshold Voltage (V_{TH}), Inverse Subthreshold Slope (SS), and low field mobility (μ_0) are presented and discussed.

3. Device Characteristics

The n-channel Ω-gate nanowires were fabricated at CEA-Leti in France, using SOI wafers featuring a buried oxide thickness of t_{BOX}=145nm [4]. In Figure 1, a schematic 3D representation of a nanowire transistor is depicted, showcasing its key geometric characteristics. The silicon film remains intentionally undoped. The gate stack consists of an interfacial SiO2 layer succeeded by a 2.3 nm thick HfSiON layer, a 5 nm TiN metal gate, and a 28 nm polysilicon layer. All devices exhibit a fin height (H_{FIN}) of 9 nm and employ a multi-fin design with 10 parallel fins, with a constant channel length (L) of 100 nm, and variable fin width (W_{FIN}) of 10, 15, 20, 40, and 60 nm.

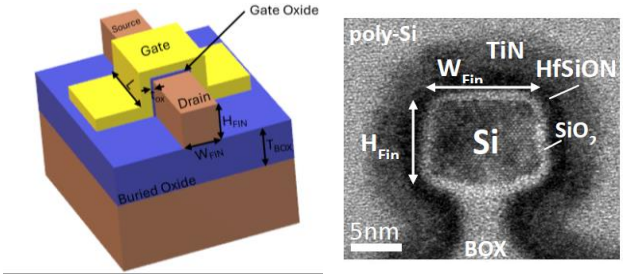

Fig. 1 *3D view of the Ω-gate nanowire, indicating their main geometric parameters.*

4. Experimental Results

The drain current (I_{DS}) versus gate voltage (V_{GS}) curves were measured with temperatures ranging from 82 K to 350 K, utilizing a Low-Temperature Microprobe (LTMP) system from MMR Technologies and a B1500A Semiconductor Parameter Analyzer. The devices were biased with a low drain voltage (V_{DS}) of 25mV.

A. Threshold Voltage

The Threshold Voltage (V_{TH}) was determined using the double derivative method [5] for all devices and temperatures. Fig. 2 illustrates V_{TH} as a function of temperature for transistors with L=100 nm and varying W_{FIN}. As expected, V_{TH} decreases with increasing temperature, as indicated by the rates provided in Table I. These results highlight the diminishing dV_{TH}/dT with decreasing W_{FIN}. Moreover, increasing W_{FIN} leads to V_{TH} degradation due to reduced electrostatic immunity.

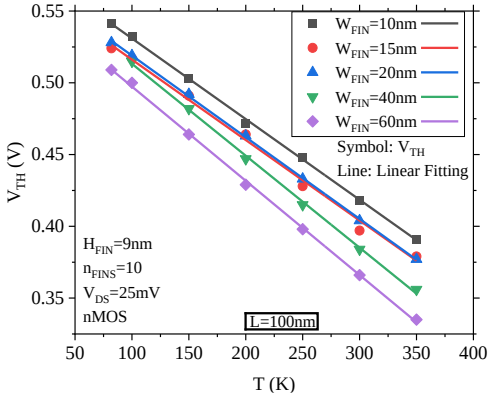

Fig. 2 *Threshold Voltage (V_{TH}) as a function of Temperature for different W_{FIN} and L = 100nm.*

Table I *dV_{TH}/dT for different W_{FIN}*

dV_{TH}/dT for different WFIN	
W_{FIN} (nm)	dV_{TH}/dT (mV/K)
10	-0.56
15	-0.56
20	-0.57
40	-0.64
60	-0.66

B. Inverse Subthreshold Slope

Fig.3 presents the inverse subthreshold slope (SS) as a function of temperature. It is possible to see that SS almost increases linearly with the temperature, regardless of the temperature. SS remains close to the theoretical limit given by Eq. 1, for the narrower transistors. Where k is the Boltzmann constant, T is the absolute temperature and q is the electron charge. The subthreshold slope of the narrower nanowires is close to the theoretical limit for temperatures down to 100 K. Additional reduction in the temperature degrades the body factor due to interface traps, leading to higher subthreshold slope values than the theoretical limit at the cryogenic regime. The increase in the fin width slightly degrades the subthreshold slope in the whole temperature range.

$$k \times T \times \ln(10)/q \qquad (1)$$

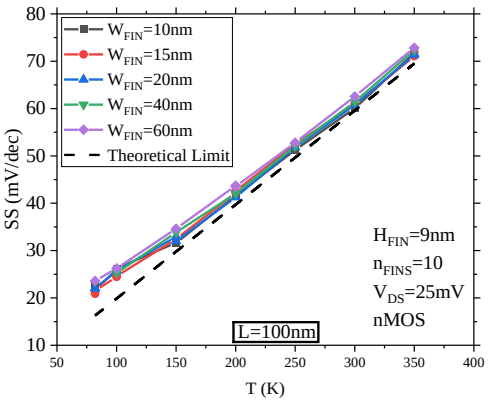

Fig. 3 *Inverse Subthreshold Slope (SS) as a function of temperature for transistors with different W_{FIN} and L = 100nm.*

C. Low-Field Mobility

Applying the Y-Function Method [6] in the I_{DS} versus V_{GS} curves, it was possible to extract the low-field mobility (μ_0). Fig 4 shows the μ_0 as a function of temperature. The μ_0 decreases with temperature increase for all transistors. and the variation with W_{FIN} is negligible across the entire temperature range for all transistors except the nanowire with W_{FIN} = 60nm. This device demonstrates consistently lower μ_0 across all temperatures, with the difference μ_0 compared to other devices, decreasing as the temperature rises.

In the temperature range being studied, carrier-carrier and neutral impurity scattering can be considered negligible. Consequently, phonon scattering emerges as the primary mechanism affecting mobility with temperature. Phonon scattering arises from the interaction between carriers and the crystal lattice, which undergoes heightened vibrations as temperature increases, thereby exacerbating mobility degradation.

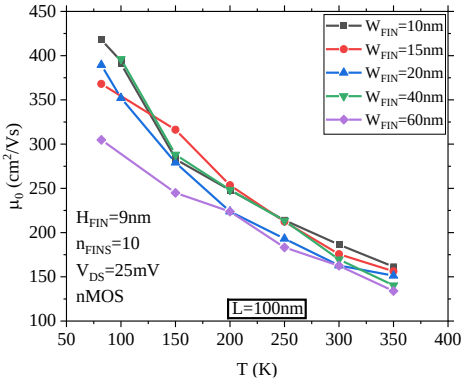

Fig. 4 *Low-field mobility as a function of temperature for transistors with different W_{FIN} and L = 100nm.*

5. Conclusion

This work presented the electrical characterization properties of Ω-gate SOI nanowires with L=100nm and variable W_{FIN}, in the 82 K to 350 K temperature range.

The threshold voltage variation with temperature increases with the fin width. Comparing the rate dV_{TH}/dT for the narrower and wider devices, an increase of 17 % is found.

Nanowires show SS near to theoretical minimum down to 100 K, but lower temperatures increase interface traps, surpassing the theoretical limit. Wider fins slightly degrade in the whole temperature range.

The low field mobility exhibited a decrease in mobility with increasing temperature for all transistors. The phonon scattering mechanism emerges as the primary mechanism affecting mobility, in the whole range of temperatures.

Acknowledgments

The authors would like to thank CNPq and FAPESP (grants #2019/15500-5 and #2022/14874-1) for the financial support during the execution of this work.

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Performance of Stacked iFinFET, GAA FET, FinFET through 3D TCAD Simulation

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1. Abstract

This work examines the performance of stacked-channel devices, specifically iFinFET (Inserted-oxide FinFET) and GAA FET (Gate All Around FET), alongside conventional bulk FinFET, utilizing numerical TCAD 3D simulations. Key parameters including drain current (I_{DS}), threshold voltage (V_{TH}), Subthreshold Slope (SS), Drain Induced Barrier Lowering (DIBL), and Transconductance (g_m) are simulated and compared to assess the superiority of stacked-channel devices over FinFET.

2. Introduction

Due to the large-scale reduction of integrated circuits, the planar MOSFET transistor reaches its limit in physical reduction and performance. The proposal for a channel in the form of a vertical fin or stacked channels then emerged (Fig. 1a), bringing promising solutions that have recently advanced successfully in several aspects [1]. From this technological improvement, the gate-all-around (GAA) FET structure (Fig. 1c) can provide greater electrostatic integrity [2] and is therefore expected to be adopted eventually in future generations of CMOS technology [3]. On the other hand, without increasing complex production cost to reduce the vertical NW spacing, inserted-oxide FinFET (iFinFET) is proposed (Fig. 1b). This i-oxide provides improved capacitive coupling between the gate electrode and the NW channel regions, bringing the electrostatic integrity of the iFinFET closer to the NWFET.

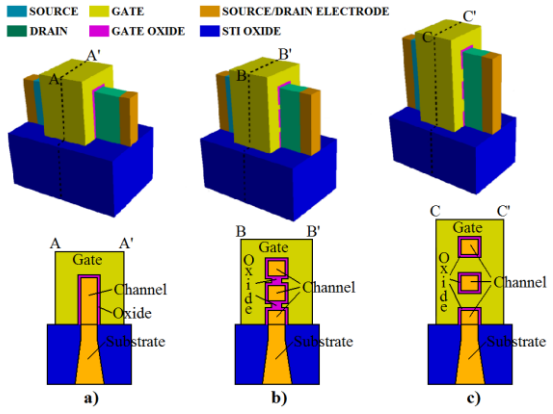

Fig.1: Structure and schematic representation of the channel cross section for: a) FinFET, b) iFinFET and c) GAA FET.

The promising results of the investigated electronic parameters such as Drain/Source current (I_{DS}), Threshold Voltage (V_{TH}), Subthreshold Slope (SS), Drain Induced Barrier Lowering (DIBL) and Transconductance (g_m) will support the proposal of stacked-channel devices.

Three-dimensional physical characteristics of the devices is depicted in Fig. 1a. The cross-section of each device is presented in Figure 1a) - FinFET, 1b) - iFinFET and 1c) - GAAFET, whose dimensions are provided in Table I.

Table I. Transistor Design Parameter Values Simulated.

Device Parameter	FinFET	iFinFET	GAA FET
L (nm)	12	12	12
H_{Fin} (nm)	18	6+6+6	6+6+6
W_{Fin} (nm)	6	6	6
Gate T_{ox} (nm)	0.7	0.7	0.7
Inserted Oxide Height (nm)	0	3.2	0
Channels Spacing (nm)	0	3.2	6
W_{Fin}*H_{Fin} (nm^2)	108	108	108

3. Simulation Setup

The fig. 2 shows the experimental data presented in the literature were used to validate our TCAD models and simulations [4].

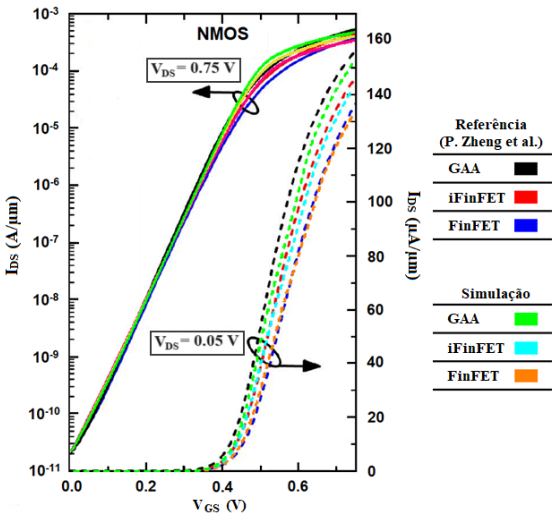

Fig.2: Calibration of reference [4]

Considering data from table I and also important parameter such as: mobility, doping, models and materials statements, the simulations were adjusted. For both cases, one can see good agreement between simulated and measured data. Source and drain used a concentration of $2x10^{20}$ cm^{-3} and for the channel $5x10^{15}$ cm^{-3}. Drain leakage current was adjusted to 20 pA/µm in the off state.

4. Results and Discussion

Fig. 3 shows the maximum drain current for each structure when the gate voltage reaches 0.75 V and the gate length ranges from 10 nm to 20 nm and drain voltage is fixed at 0.75 V. It is seen that, as expected, with the increase of channel length the I_{DSmax} decreases for all devices.

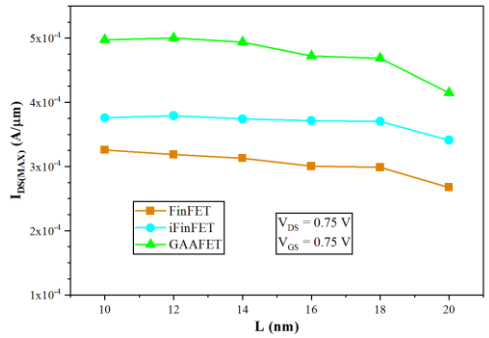

Fig.3 $I_{DS(max)}$ for FinFET, iFinFET and GAAFET devices.

The behavior of V_{TH} is presented in Fig. 4. Stacked GAAFET exhibits lower V_{TH} and nearly ideal SS (Fig. 5) in devices with channel length (L) >= 16 nm; this fact occurs because these devices also exhibit better short-channel properties.

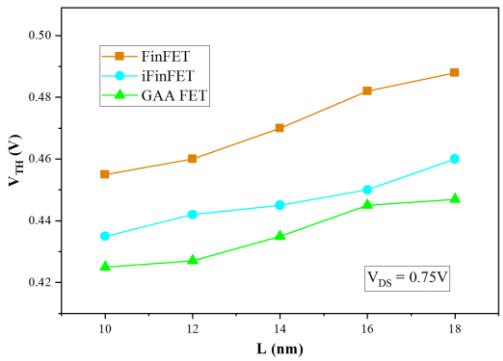

Fig.4 V_{TH} for 3D Stack Channel Devices.

Fig. 6 presents the g_m and DIBL. It can be observed that as the channel length increases, DIBL is much lower in all stacked devices. The maximum transconductance describe the field effect transistor gain and is given by the derivative of the I_{DS} to the V_{GS} [$g_m=\partial I_{DS}/\partial V_{GS}$] and the g_m of each device is displayed in Fig. 6. The structure who has the higher I_{DS} conduced (GAA FET) must have the higher g_m (GAA FET) for same L and V_{DS}.

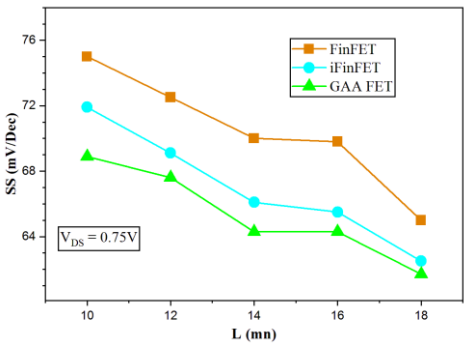

Fig.5 SS for FinFET, iFinFET and GAAFET devices.

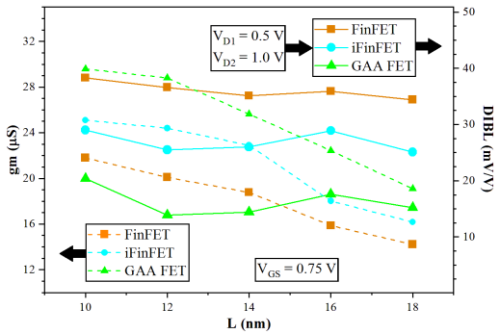

Fig.6 g_m and DIBL for 3D Stack Channel devices.

5. Conclusions

In this paper, the performance of the stacked-channel structures over the single-channel structure was studied. The simulation results demonstrate that structures with multi-cannels or stacked channels (GAA FET and iFinFET) have better performance compared with single-channel structure (FinFET) in all simulated parameters. This is linked to the larger contact surface of the gate in relation to the channel (>W_{eff}), which implies an increase in gate/channel electrostatic coupling and a higher I_{DS} for the same active region area (W_{Fin}*H_{Fin}). Thus, it is evident from the simulation that stacked channel structures offer greater advantages over the single channel structure with substantial replacement potential for future integrated semiconductor devices.

Acknowledgments

Thanks to FAPESP (Process Nº: 2023/00123-7).

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Extraction of the Effective Channel Length of Junctionless Nanowire Transistors Through Capacitance Characteristics for Different V_{DS} Bias.

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Abstract – This paper presents an analysis of the effective channel length (L_{EFF}) of Junctionless nanowire transistors (JNT) through the gate capacitance (C_{GG}) when its drain is biased. The study has been done considering different channel and source/drain lengths, as well as different doping concentrations (N_D) and structures with lateral spacers, showing that the L_{EFF} is longer than channel mask length (L_{MASK}) in all conditions and presents some dependence with V_{DS} and N_D.

I. Introduction

This analysis studied the Junctionless Nanowire Transistor (JNT) in Silicon on Insulator (SOI) technology, which is similar to an accumulation mode transistor, i.e., when it is in the off state, no current flows through its channel because the device's channel is completely depleted due to the work function difference between the gate and channels materials. However, when the gate is biased, overcoming the threshold voltage, one current component appears, flowing by the center of the channel, and is called body current (I_b) [1-5].

When the gate voltage (V_{GS}) increases, reaching the flat band voltage (V_{FB}), an accumulation stack is formed next to the junction of the channel silicon and gate oxide, originating a new current component due to the electrons' flow through an accumulation layer (I_{acc}) [6].

The JNT brings a noticeable improvement if compared to the bulk and SOI MOSFET mainly because of the absence of the dopants type variation between the source/channel/drain regions, which promotes a reduction in manufacturing difficulty as well as a reduction in the short channel effects (SCEs) and allows for a better integration scale [1-4].

An important feature of this device is that its effective channel length is longer than the mask channel length for the structures featured with lateral spacers [7-9]. Up to now, only a few papers treating this phenomenon physics' and methods proposing to extract the effective channel length of experimental devices can be found in the literature. So, this work aims to evaluate the method proposed in [8], extending its application for different drain biases.

II. Structure characteristics.

The structure used in this work is similar to the one presented in [7-9] and consists of a tri-gate Junctionless Nanowire Transistor in SOI technology with channel mask length (L_{MASK}) varying from 30 to 100nm, nanowire height (H) of 10nm, width (W) of 20 nm, effective gate oxide thickness (EOT) of 1.5 nm, buried oxide (T_{box}) of 150 nm, doping concentration (N_D) of $5x10^{18}$ cm^{-3} and $1x10^{19}$ cm^{-3} and source and drain (L_{SD}) varying from 5 to 30nm with lateral spacers along the entire L_{SD} similarly as presented in fig 1.

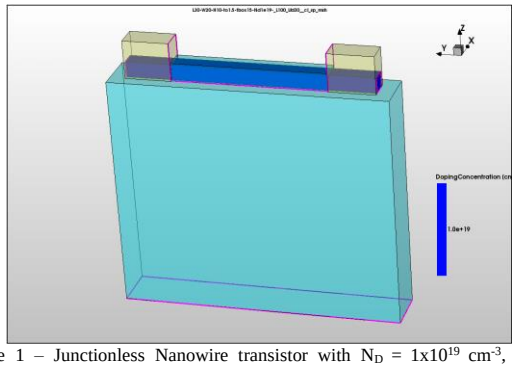

Figure 1 – Junctionless Nanowire transistor with N_D = $1x10^{19}$ cm^{-3}, L_{MASK} =100nm, L_{SD} = 30nm and lateral spacer.

This structure was simulated using the 3D numerical simulations in Synopsys Sentaurus [10]. All the JNT simulations have considered the drift-diffusion transport mechanism, generation and recombination, mobility dependence on the lateral electric field, and bandgap narrowing models. The simulations were validated by experimental data as presented in Fig 2 with the C-V curve of a JNT provided by CEA-LETI [11].

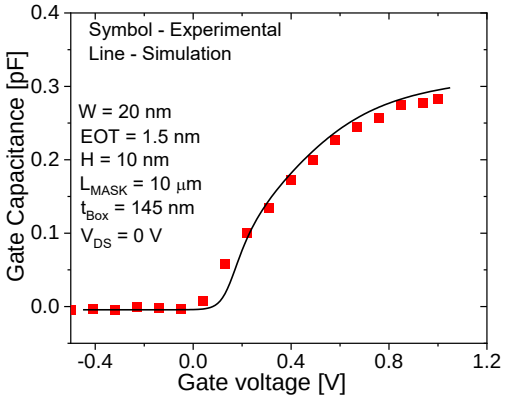

Figure 2 – Experimental validation of the gate capacitance as a function of gate voltage compared to the simulated structure.

III. Analysis and results

The use of gate capacitance (C_{GG}) is a good way to extract the effective channel length of the devices (L_{EFF}) when it is in accumulation mode with low drain voltage (V_{DS}) as presented in [8].

The gate capacitance (C_{GG}) as a function of V_{GS} for V_{DS} = 0.5 and 1V is presented in Figs 3 and 4 where one can see the phenomenon of intersection in the curves, which represents the bias where the devices are in the pinch-off condition. At this point, capacitance presents no dependence on V_{GS}, enabling the extraction of the effective channel length using the method presented in [8]. which is based on the gate capacitance curve in the pinch-off point as a function of L_{MASK}, and then, its extrapolation to the zero-capacitance value. The obtained value consists of a negative L_{MASK}, which represents the variation in the channel length (ΔL) as presented in Fig 5 and is around 4~6 nm.

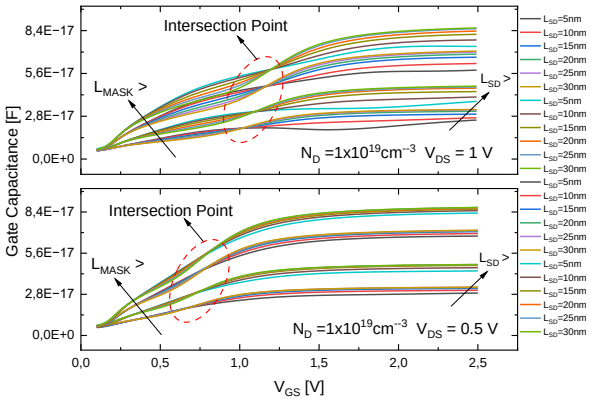

Figure 3 – Gate capacitance as a function of V_{GS} for N_D of $1x10^{19}cm^{-3}$and both V_{DS}.

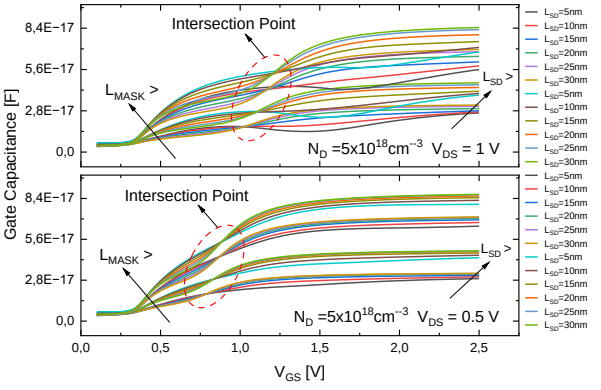

Figure 4 – Gate capacitance as a function of V_{GS} for N_D of $5x10^{18}cm^{-3}$and both V_{DS}.

4. Conclusions

Along the work, it was possible to apply a capacitance-based methos to extract effective channel length of JNT with different biasing conditions. It was possible to notice that L_{EFF} increases for both considered V_{DS} biases when the device is in the pinch-off condition regime for all structures as well as the L_{EFF} value is around 4 to 6 nm and presents some dependence with V_{DS} and N_D.

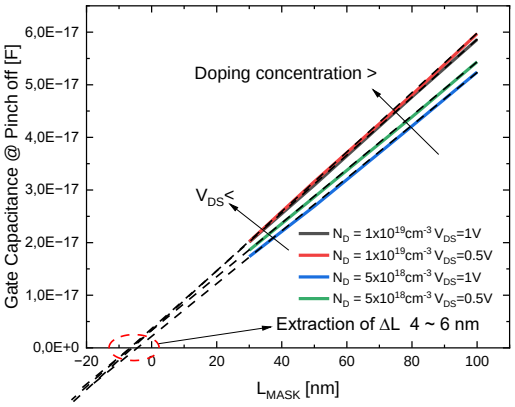

Figure 5 – Gate Capacitance (@pinch_off) as a function of L_{MASK}.

Acknowledgments

This work was supported by São Paulo Research Foundation (FAPESP) grant #2019/15500-5, National Council for Scientific and Technological Development (CNPq) grants #303938/2020-0, #427975/2016-6, #406193/2022-3, #311892/2023-0 and financed in part by the Coordenação de Aperfeiçoamento de Pessoal de Nível Superior - Brasil (CAPES) - Finance Code 001.

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Evaluation of Threshold Voltage Extraction Methods in SOI Nanowires Transistors as a Function of Temperature.

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1. Abstract

This work presents a comparative analysis of eight threshold voltage extraction methods applied to SOI nanowire transistors. For that, experimental data and three-dimensional simulations were obtained for long-channel transistors with two different channel widths at temperatures. From the simulations, the physical value of the threshold voltage was extracted and used as a reference to compare the methods. It was observed that the transconductance-to-current method presents the best correspondence with the adopted physical value.

2. Introduction

Nowadays, the demand for electronic devices of ultra-low power consumption has increase, mainly due to Internet of Thing (IoT) [1] growth. To reduce the power consumption of a transistor, it is necessary to decrease the threshold voltage (V_t), so the supply voltage can also be reduced. This parameter is one of the most important to model a MOSFET [2] since it defines the necessary voltage to turn the transistor on. So, it is important to define its exact value to design an electronic circuit correctly. In the literature, there are many methods to extract the threshold voltage, each of them presenting different results for the same device, showing an uncertainty about the exact value. For planar transistor, the threshold voltage is defined as the gate voltage that raises the surface potential of the channel to two times the Fermi potential. However, in undoped body devices, such as nanowires, this definition is not valid since a considerable current level is observed even in weak inversion. In these cases, the most suitable definition for V_t is the gate voltage that equals the diffusion and drift current components.

The nanowire tri-gate SOI MOSFET improves the electrostatic gate coupling, reducing short-channel effects (SCEs) [3], constituting a promising device for continuing CMOS technology scaling. A schematic representation of a nanowire transistor is presented in Figure 1, indicating nanowire width (W_{FIN}), height (H_{FIN}), and length (L).

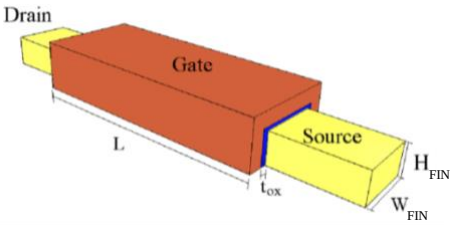

Fig.1. *Schematic view of a nanowire transistor.*

This paper aims to present an experimental and simulated comparison of eight different threshold voltage extraction methods applied to SOI nanowire transistors with different channel widths and temperatures of operation, comparing the values with a physical definition of the parameter extracted by simulations.

3. Threshold Voltage

In this work, the eight analyzed methods are based in the transistor operating in linear region. Therefore, experimental and simulated I_D vs. V_{GS} curves were obtained at V_{DS} of 40 mV. The following methods were selected [4]: the constant-current method (CC), second derivative method (2D), linear extrapolation method (ELR), transconductance linear extrapolation (GMLE), transition method (G1), ratio method (or Y-Function), second derivative logarithm method (2DL) and transconductance-current method (G_M/I_D).

Electrical measurements were made on chips fabricated by CEA-Leti [5]. The gate stack is composed of a thin interfacial SiO2 layer, followed by 2.3 nm HfSiON, 5 nm TiN, and 50 nm polysilicon. The effective oxide thickness (EOT) is around 1.4 nm. The channel region is not intentionally doped. All devices present a fin height of 9 nm, channel width of 10 nm and 40 nm and channel length of 100 nm. The drain current curves as a function of the gate voltage were extracted using the microprobe system from MMR Technologies, which heated the devices from 300 K to 550 K.

The three-dimensional simulations were made using Sentaurus Device Simulator, with the same dimensions, bias voltages and temperature as the experimental analysis. In the simulations, the physical value of V_t was also extracted, by finding the gate voltage where diffusion and drif currents are equal, to use as a reference to the other methods.

4. Results and Discussion

The threshold voltage as a function of temperature is presented in Figure 2 for W_{FIN} = 10 nm and 40 nm and L = 100 nm. As can been seen, the methods present different values, indicating the dependence of the value of V_t on the extraction method. However, all methods present a linear decrease with the temperature increase.

To analyse if the variation is the same for all methods, the dV_t/dT as a function of W_{FIN} is shown in Figure 3. From these results, it is possible to see that dV_t/dT shows a slight dependence on W_{FIN} independent of the method. On the other hand, the extraction method significantly

impacts the measured dV_t/dT. The G_M/I_D presented the smallest slope, which is, on average, approximately half of the highest, obtained by the CC method.

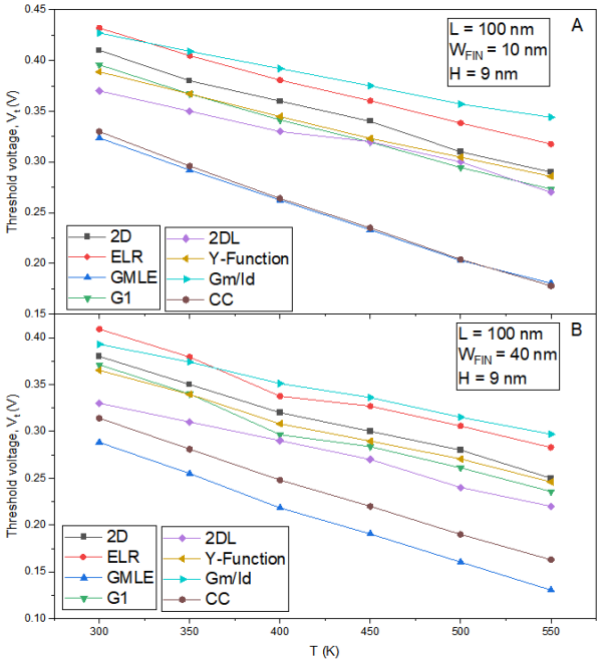

Fig.2. *Vt as a function of T for L = 100 nm and (A) W_{FIN} = 10 nm, (B) W_{FIN} = 40 nm of experimental data*

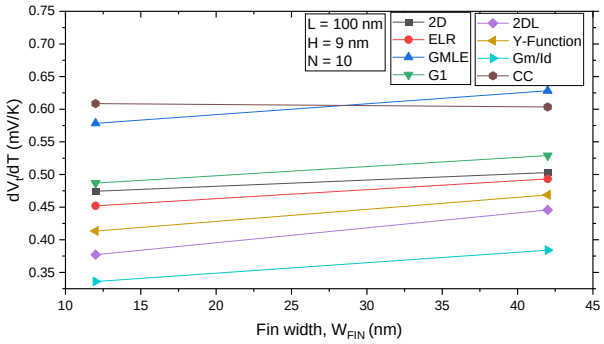

Fig.3. *Slope as a function of W_{FIN} of experimental data.*

In Figure 4 it is shown the simulated results of threshold voltage extracted by the eight methods and by the physical definition. Is possible to see same linear tendence as the experimental data. Besides that, it is possible to see that the G_M/I_D method presents a good match with the definition of threshold voltage in all range of temperature and both channel width.

Analysing the dV_t/dT vs W_{FIN} from the simulations in the Figure 5, it is possible to see that the G_M/I_D is the only the method which presents the same values of physical definition, while the others present a higher value, reaching almost the double in the GMLE method.

5. Conclusions

This paper presented an analysis of different threshold voltage extraction methods based on drain current curves using experimental and simulated data of SOI nanowires transistor with long channel. It was shown that V_t is highly dependent on the extraction method. From the three-dimensional simulations, it was possible to extract the physical value of V_t and compare with the methods, showing that the G_M/I_D method is the most suitable for long channel devices, since both value and slopes were similar in the analysed range of temperatures.

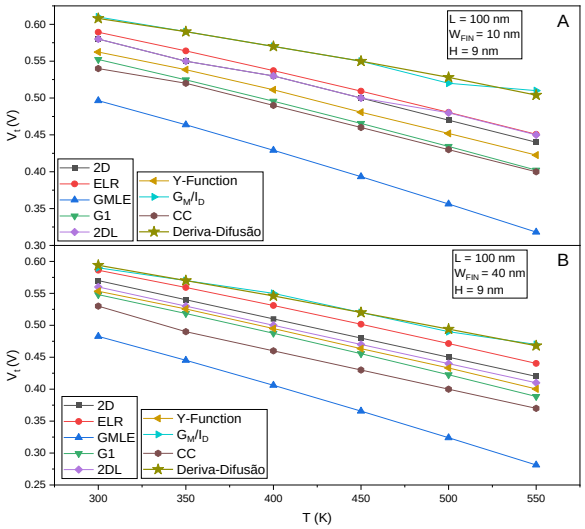

Fig.4. *Vt as a function of T for L = 100 nm and (A) W_{FIN} = 10 nm, (B) W_{FIN} = 40 nm of simulated results.*

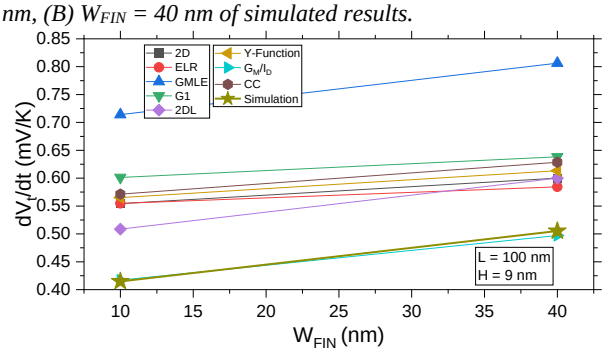

Fig.5. *Slope as a function of W_{FIN} of simulated results.*

Acknowledgments

The authors acknowledge FAPESP for the financial support to this work (Grants number 2022/12622-5) and thank CEA-Leti for providing the devices used in this work.

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Comprehensive Evaluation of Junctionless and Inversion-Mode Nanowire MOSFETs' Electrical Characteristics at High Temperatures

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1. Abstract

This work aims to comprehensively compare the electrical properties of junctionless and inversion-mode nanowires MOSFETS, fabricated with similar gate stack and state-of-art process, in the temperature range from 300 K to 580 K. The comparative analysis is performed through the main electrical parameters of the devices, such as the threshold voltage, subthreshold slope, conduction current and mobility extracted from experimental data. Devices with different fin widths are compared.

2. Introduction

The increase in power density in integrated circuits due to the increase in the number of transistors operating simultaneously driven by the scaling process of MOS technology leads to the intensification of heating processes. Moreover, there are some applications in which the external environment where the circuit is inserted causes its heating. These applications include sensors coupled to automotive engines that can reach 200º C, sensors coupled to petroleum exploration probes whose temperature can reach 175º C, and aerospatial industry applications [1]. Hence, understanding how temperature increases influence the electrical properties of the devices composing the state-of-the-art electronics industry is fundamental to projecting devices and circuits that are more robust to thermal variation.

The objects of study of this work are the triple-gate nanowire transistors of two types, the inversion-mode and junctionless nanowire transistors. They are an alternative for the MOSFET downscaling, and their gate geometry provides excellent control of the channel charges, mitigating short channel effects,

The inversion-mode nanowire transistor (IM) has opposite dopant types in the source/drain and channel regions. When the gate voltage achieves the threshold voltage (V_{TH}), the silicon layer is completely depleted, and an inversion layer is formed in the top and side gate oxide-silicon interfaces [2]. The junctionless nanowire transistor (JNT) has the same dopant type in the silicon layer, and the difference in work function between silicon and the metal gate initially turns it off. When the gate voltage achieves the threshold voltage, it starts conducting through the center of the device, where a neutral channel is formed. When the gate voltage achieves the flat band voltage, the entire silicon layer is neutral, and an accumulation layer appears for higher applied gate voltages.

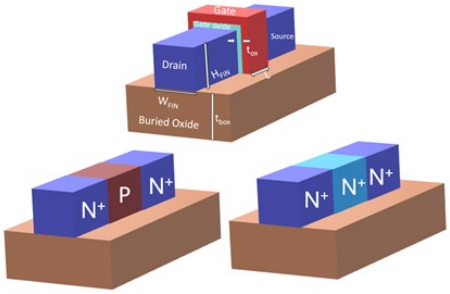

Fig.1. *Schematic diagrams of the structure of IM nanowire transistor (left) and JNT nanowire transistor (right).*

3. Devices Characteristics

The IM and JNT nanowires studied in this work were fabricated in CEA-Leti, in Silicon-On-Insulator (SOI) substrates. The buried oxide has a thickness of 145 nm. Also, both devices have ten parallel fins, fin height H_{FIN} of 9nm, channel length L=100nm, equivalent gate oxide thickness of 1.3 nm, and n-type doping concentration in the source/drain regions of $N_D = 5x10^{20}$ cm^{-3}. The transistors have fin width W_{FIN} of 10nm, 15nm, 20nm, and 40nm. The JNTs channel region is heavily doped n-type silicon with doping concentration $N_D=5x10^{18}$ cm^{-3}. The IM nanowires channel region is lightly-doped (or not intentionally doped) p-type silicon with a concentration of $N_A=1x10^{15}$ cm^{-3}.

4. Experimental Results

The I_{DS} x V_{GS} curves were experimentally measured from 300 K to 580 K through a Low-Temperature Microprobe (LTMP) system from MMR Technologies and a B1500A Semiconductor Analyzer. Figure 2a shows the measured drain current in the function of gate voltage in linear and logarithmic scales for the junctionless and inversion-mode nanowire transistors with W_{FIN} of 10 nm at drain voltage (V_{DS}) of 25 mV and different temperatures.

The threshold voltage of both devices was extracted through the g_M/I_{DS} method, where g_M is the transconductance. Fig 2b shows the average value of V_{TH} extracted from 3 measurement sets in the function of the temperature of both devices. The IM nanowire transistors presented a higher variation of V_{TH} with

temperature due to the higher dependence of the Fermi potential of IM devices on temperature, which is dependent on the bandgap E_G. The bandgap narrowing occurs in both devices due to temperature. However, the JNT has a more intense bandgap narrowing due to higher doping concentration in the channel [3].

The inverse subthreshold slope (SS) is the inverse of the slope of the linear region in the subthreshold region (low gate voltage) in the semilogarithmic scale of the I_{DS} x V_{GS} curve. It depends on the body factor and thermal potential kT/q, where k is the Boltzmann constant. The average inverse SS of both devices with different W_{FIN} is shown in Fig 2c and Fig 2d.

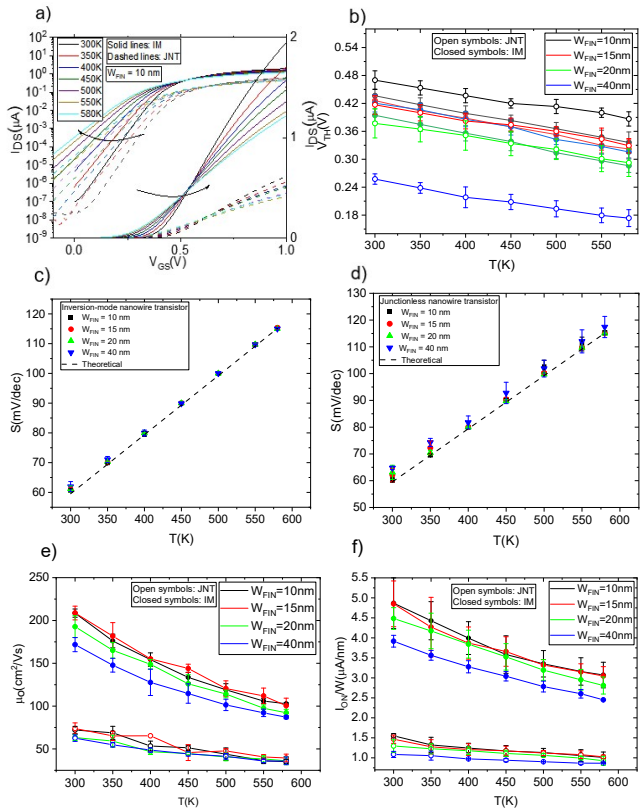

Fig.2. *a) I_{DS} x V_{GS} curves for W_{FIN} of 10 nm for different temperatures. b) Threshold voltage in the function of temperature. c) Inverse SS of IM transistors in function of temperature. d) Inverse SS of JNT transistors in the function of temperature. e) Moblity of both devices in function of temperature. f) Conduction current of both devices in function of temperature.*

Both devices presented a variation of the inverse SS with a temperature of 0.197 mV/decK, which is very close to the theoretical limit of 0.199 mV/decK. This shows the better electrostatic control the triple gate nanowire transistors provide and its immunity against short-channel effects.

The low-field mobility of both transistors was extracted through the Y-function method. Fig 2e shows the transistors' low-field mobility in the temperature function. There is a gain of mobility at low temperatures due to less lattice vibration. However, for JNT devices, the neutral impurities scattering counterbalances this gain due to their higher doping concentration in the channel. For this reason, the JNT transistors presented less mobility variation with temperature, although they presented lower mobility values. To quantify the mobility variation with temperature, it was extracted the temperature coefficient α since $\mu \propto T^{\alpha}$[4].

The conduction current was extracted at a gate overdrive voltage of 0.4 V and V_{DS} of 0.9 V to compare the current of both devices in the same operating conditions. The conduction current variation with temperature depends on the threshold voltage variation and the mobility variation with temperature. As the I_{ON} was extracted at a fixed overdrive voltage, the variation of V_{TH} with temperature does not influence its variation. Hence, the I_{ON} variation with temperature follows the mobility variation with temperature for both devices, as shown in Fig 2f.

Table 1 summarizes the variation of each parameter with temperature for both devices with a W_{FIN} of 10 nm.

Table 1: Comparison of the variation of parameters with temperature of both devices.

W_{FIN}=10 nm	Junctionless	Inversion-mode
dV_{TH}/dT (mV/K)	-0.29	-0.35
dSS/dT(mV/dec*K)	0.197	0.197
α (μ_o coefficient)	-1.088	-1.093
dI_{ON}/dT(μA/K)	-1.51	-6.66

5. Conclusions

From the experimental data analysis, it's possible to conclude that the IM nanowire transistors perform better than JNT in terms of the parameters analyzed. However, the JNT nanowire transistors have higher thermal stability with less variation of the parameters with temperature than the IM nanowire transistors, with a 17% lower variation of threshold voltage, a 22% lower temperature coefficient for mobility, and a 77% lower variation of conduction current with temperature for fin width of 10 nm.

Acknowledgments

The authors would like to thank Capes, CNPq and FAPESP (grant #2019/15500-5) for their financial support during the execution of this work.

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Zero stress and mass loading packages for SAW based lab-on-chips

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1. Resume

Assembling of the surface acoustic wave (SAW) based microfluidic lab-on-chips (MLC) has a stage of attachment of the microfluidic cell (MC), which plays a role of the package for such devices, to the surface of piezoelectric substrate. Due to unavoidable technical limitations, interdigital transducers (IDT), which irradiate SAWs, are placed, normally, outside the MC. Thus, the SAW, passing under the walls of the MC, suffers significant insertion lose and heats them for up to 5-10 degrees, that is unacceptable for majority of applications. We show that it is possible to eliminate or, at least, dramatically minimize these losses without compromising the ability to confine the liquid inside the MC by controlling mechanical stress applied to MC and by attaching it to the crystal only in specific parts, which don´t interact with the SAW. The proposed method of packaging opens the possibility to perform operations, which require high acoustic energy level inside active area of the MC.

2. Introduction and theoretical background

SAW based MLC present the class of MEMS, mounted on the surface of a strong piezoelectric, which uses acoustic waves for different purposes. Using SAW it is possible to move droplets, sort different cells, monitor dynamic of different chemical reactions inside the MLC among other things [1]. All MLCs use MCs, normally made of polymer silicon as the principal element in the way similar to the package of the traditional microchip is used. Due to various technical limitations, interdigital transducers (IDT), which generate SAWs, should be placed outside the MC. Thus, packaging of such device present a significant challenge because attachment of the MC to the surface of a crystal should guarantee minimum interaction between the SAW and the MC to avoid excessive insertion loss (IL). Typical situation is shown in the fig. 1. The SAW, generated by IDTs (1), reaches the MC (2), crosses its walls and reaches the working area of the MC (3), where mixing of droplet components take place.
To do such operations, the SAW should have significant (up to 5W) power. Considering small size of the working area, such energy can cause significant heating of the working area, which is unacceptable for majority of applications.

The mechanism of such a high IL could be explained by the analysis of interaction of the SAW with the wall of the microfluidic cell shown in the fig. 2.

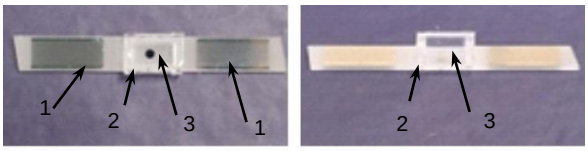

Figure 1. Simple SAW based MLC. IDTs, which generate the SAW (1); microfluidic cell attached to the surface of the MLC (2); working area of the MLC (3).

According to it, when the incident SAW (1) reaches the wall of the MC (8) it splits into the propagating SAW (2), reflected SAW(3), bulk acoustic wave (BAW) , which enters inside the wall of the MC(4) and goes inside a crystal (5). It is the area of the contact (AC) (7), which determines all these energy transformations and, hence, the heating of the MC and losses. Total losses in such an interaction can reach 10 dB, leaving only 10% of initial energy for useful transmitted wave (2) and 90% for heating.

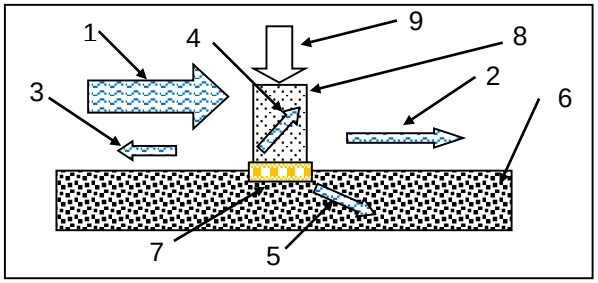

Figure 2. Process of interaction of the SAW with the wall of the microfluidic cell. 1 – Incident SAW; 2 - Transmitted SAW; 3 – Reflected SAW; 4 (5)– BAW, which propagate inside a polymer wall (crystal); 6 – Piezoelectric crystal; 7 – Area of the contact between the crystal and the polymer wall; 8 - Polymer wall; 9 – External force (load) applied to the top of the wall

It is the mechanical stress and mass loading in AC, which determine energy transformation. In this paper, we studies in details of interaction of the SAW with MC walls and propose the simple way of packaging, which reduce this kind of losses practically to zero without loss of microfluidic functionality of MLC.

3. Experimental measurements and discussion

For testing of the interaction of the MC with the SAW

special delay line (DL) with two fan-shaped IDTs (FIDT) was fabricated (see fig. 3). FIDT (1) can be treated as a set of separate sub channels each of which generates its specific frequency [2]. If a block of polymer (2), which represents the wall of MC, is placed inside this DL, it interacts with frequencies of SAW from f_3 to f_4, inserting additional IL in this frequency band. This IL was measured with the network analyser and the experimental results are shown in fig. 4 (green and red curves). Red curve 9 dB drop for $f_3<f<f_4$ is attributed to this effect.

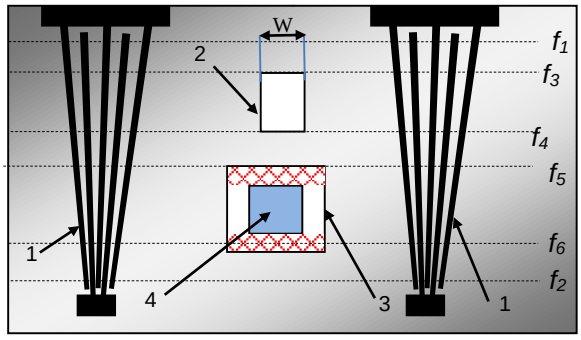

*Figure 3. SAW delay line with fan-shaped IDTs (1). Horizontal dashed lines correspond to different frequencies. $f_1(f_2)$ – minimum (maximum) frequency of the delay line; $f_3<f<f_4$ – frequency band, which corresponds to the aria overlapped by the placed polymeric block; f_5 and f_6 – frequencies, which correspond to channels covered with glue marked with red hatched areas. 2 – polymer block of width **W** placed on the surface of the crystal; 3 – microfluidic cell glued to the surface of the crystal by hatched areas; 4 working area of the MC*

Experimental tests show that IL increase and heating occur mainly into AC (7) (see fig. 2). Special fixture, which allows applying different load to the MC was developed and IL increase was measured experimentally

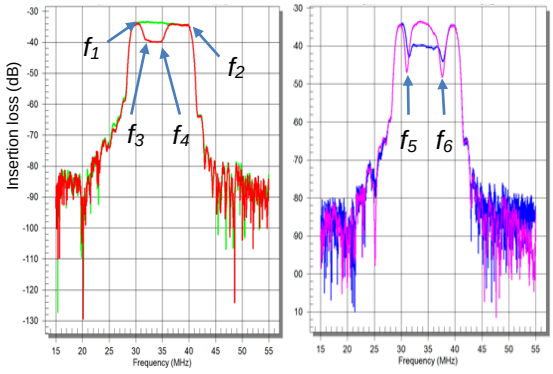

Figure 4. Experimental results of measuring of the insertion loss of the DL in various conditions. Green curve – IL of the empty DL; Red – IL of the DL with placed polymer block; Blue – IL of the DL with microfluidic cell glued by entire perimeter; Magenta - microfluidic cell glued by hatched area of the fig.3.

(see fig. 5). The results show that it is possible to arrange conditions at which the IL is small but the MC is fixed mechanically, which allows one to use the MLC.

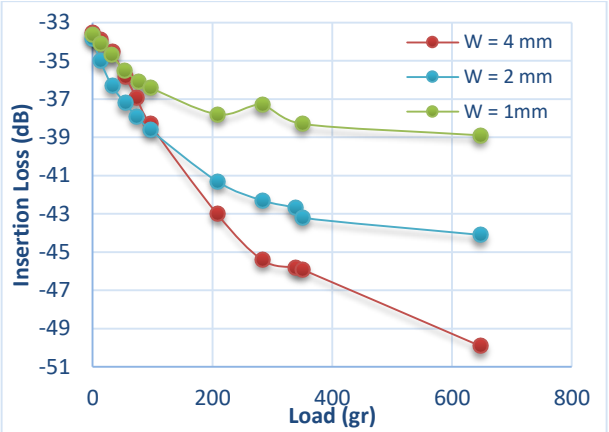

Figure 5. Experimental results of measurement of the IL caused by polymer blocks of different width W as a function of applied external force (see fig. 1)

To test the obtained result rectangular MC (see (3) in fig. 3) was assembled. In contrast to fully glued MC (blue curve in fig. 4) the assembled MC (magenta curve), which has glue only on the hatched area in the fig.3 and does not have any additional loading, does not represent any additional loss for the area which corresponds to for $f_5<f<f_6$. It means that the SAW of any power can pass though such a package without its heating. This type of packaging presents significant advantage for such MLC as biomedical cartridge, for example.

4. Conclusions

The proposed simple packaging process of SAW based MLCs resolves, without the increase of complexity, the problem of undesirable extra heating and SAW losses. It can be used for arbitrary polymer thickness and power level of the SAW. It opens the possibility to incorporate acoustic energy consuming operations with liquid in such small MLS as, for example, biomedical cartridges.

Acknowledgments

The authors gratefully acknowledge the support of the Programa de Capacitação Institucional CTI Renato Archer (PROJECT: 444303/2018-9)

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RISC-V MICROPROCESSOR ARCHITECTURE APPLICATIONS IN FPGA

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1. Abstract

This paper aims to study how to implement different applications in Field-programmable gate array (FPGA) by using the Reduced Instruction Set Computer V (RISC-V) modular microprocessor architecture. The research is divided into theoretical and practical stages, culminating in an open-source RISC-V microprocessor running on a FPGA board (DE1-SoC).

2. Introduction

The RISC-V architecture meets the recent industry demands for increasingly smaller, faster, and more versatile microprocessors, which are intended to be used in various fields, especially on personal computers, telecommunications equipment, automotive industry, medical devices, industrial machinery, video cameras, smart grids, IoT (Internet of Things) and AI (Artificial Intelligence) systems.

This work aims to study the RISC-V microprocessor architecture in two main steps. The first phase consists of theoretical research on the architecture's basic functionalities and core and modular features. The second and practical phase consists of implementing an open-source RISC-V VHDL microprocessor developed by Dr. Stephan Nolting, called NEORV32, on a DE1-SoC FPGA board, using the Quartus Prime software on a Linux Ubuntu environment.

3. NEORV32 and DE1-SoC block diagrams and RV32I core instructions

Fig. 1 illustrates the NEORV32 VHDL microprocessor top-entity block diagram [1, 2].

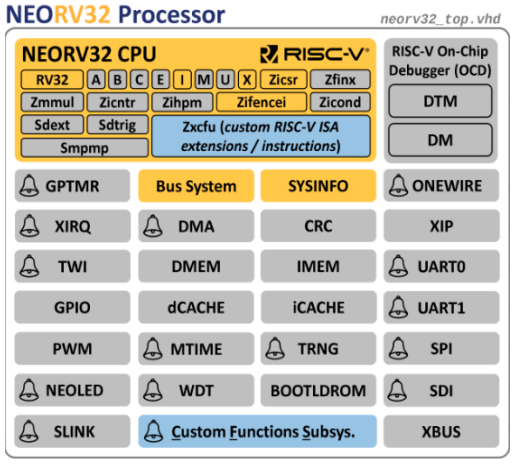

Fig. 1. *The NEORV32 processor block diagram.*

Table 1 illustrates the 32-bit formats for the 6 RV32I RISC-V core instruction types. Type-R instructions are register instructions, Type-I are for immediate values and short loads, Type-S for stores, Type-B for conditional branches, Type-U for long immediate values and Type-J for unconditional jumps [3].

Table 1. *RV32I 32-bit instruction formats.*

	31 27	26 25	24 20	19 15	14 12	11 7	6 0
R	funct7		rs2	rs1	funct3	rd	opcode
I	imm[11:0]			rs1	funct3	rd	opcode
S	imm[11:5]		rs2	rs1	funct3	imm[4:0]	opcode
B	imm[12|10:5]		rs2	rs1	funct3	imm[4:1|11]	opcode
U	imm[31:12]					rd	opcode
J	imm[20|10:1|11|19:12]					rd	opcode

Fig. 2 illustrates the DE1-SoC board block diagram [3].

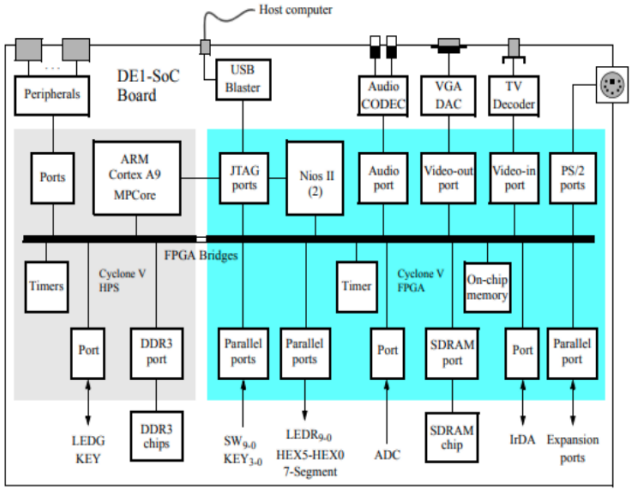

Fig. 2. *DE1-SoC board block diagram.*

4. Methodology

The methodology employed in this study involved two main stages: theoretical and practical. In the theoretical stage, the research began with an extensive literature review focusing on the RISC-V architecture's design, core, and module features. This was followed by a detailed study to understand the foundational principles of the RISC-V architecture, including its instruction set, register organization, and memory management.

In the practical stage, the implementation setup started by configuring the Quartus Prime software within the Linux Ubuntu environment and then uploading and compiling a library containing VHDL files describing features such as instruction and data memories, an UART interface, MULDIV functions, an ALU and a PWM circuit. The files also include a simplified top entity file selected for this implementation due to its suitability for the project's

objectives. Together, these files compose the NEORV32 hardware description. The microprocessor was then implemented on the DE1-SoC development board using the Quartus Prime software, and it was able to run a simple 8-bit counter written in C programming language and, using GCC, compiled to a VHDL file describing the code in machine language. This description was uploaded directly to the processor's memory, and the final result was an 8-bit counter running on the DE1-SoC board's LEDs (LEDR[0-7]).

5. Results

Fig. 3 illustrates the 8-bit counter C code that Dr. Stephan Nolting wrote [1, 2].

```c
/**********************************************************************//**
 * @file demo_blink_led/main.c
 * @author Stephan Nolting
 * @brief Minimal blinking LED demo program using the lowest 8 bits of the GPIO.output port.
 **********************************************************************/
#include <neorv32.h>


/**********************************************************************//**
 * Main function; shows an incrementing 8-bit counter on GPIO.output(7:0).
 *
 * @note This program requires the GPIO controller to be synthesized.
 *
 * @return Will never return.
 **********************************************************************/
int main() {

  // clear GPIO output (set all bits to 0)
  neorv32_gpio_port_set(0);

  int cnt = 0;

  while (1) {
    neorv32_gpio_port_set(cnt++ & 0xFF); // increment counter and mask for lowest 8 bit
    neorv32_cpu_delay_ms(250); // wait 250ms using busy wait
  }

  // this should never be reached
  return 0;
}
```

Fig. 3. *8-bit counter C code written by Stephan Nolting.*

Fig. 4 illustrates an alternative Assembly code for the same 8-bit counter [1, 2].

```asm
/**********************************************************************//**
 * @file demo_blink_led_asm/main.S
 * @author Stephan Nolting
 * @brief Simple assembly-only demo program. Implements a simple counter that
 * uses the lowest 8 bits of the GPIO's output port. The CPU cycle counter is
 * used as time base. Hence, this program requires the GPIO controller and the
 * CPU Zicsr and Zicnt ISA extensions.
 **********************************************************************/
.file "main.S"
.section .text
.balign 4
.global main

// Memory map
.set GPIO_OUTPUT_LO, 0xFFFFFC00U // address of GPIO
.set SYSINFO_CKLK,   0xFFFFFE00U // address of SYSINFO


/**********************************************************************//**
 * Entry point = main
 **********************************************************************/
main:
    li a0,  GPIO_OUTPUT_LO+8     // address of the GPIO.OUTPUT_LO register
    li a1,  0                    // clear counter

loop:
    andi a1, a1, 0xff            // mask: just keep the lowest 8 bits
    sw   a1, 0(a0)               // output current counter
    call delay                   // call delay subroutine
    addi a1, a1, 1               // increment counter
    j    loop


/**********************************************************************//**
 * Delay subroutine using mcycle (waiting for 0.25s)
 **********************************************************************/
delay:
    li   t0, SYSINFO_CKLK+0      // address of SYSINFO.CLK
    lw   t0, 0(t0)               // read SYSINFO.CLK (= CPU clock speed in Hz = tick per second)
    srli t0, t0, 2               // = ticks per 0.25 seconds
    csrw mcycle, zero            //clear cycle counter (low word)

delay_loop:
    csrr t1, mcycle              // get current cycle counter (low word)
    bltu t1, t0, delay_loop      // restart loop if mcycle < t0
    ret                          // return to main
.end
```

Fig. 4. *8-bit counter Assembly code written by Stephan Nolting.*

Fig. 5 demonstrates a simulation of the 8-bit counter in/out waveforms on a time slice.

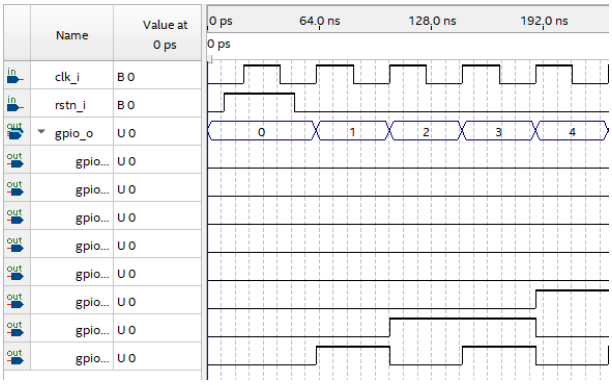

Fig. 5. *8-bit counter waveform simulation.*

6. Conclusions

The results obtained from this work were consistent with its scope. In addition to conducting a comprehensive study on the theoretical and technical aspects of the RISC-V architecture, it was also possible to verify its real-time operation through the DE1-SoC board. Additionally, for the process of uploading the NEORV32 processor to the board using the Quartus Prime tool to be successful, a thorough study of the software and its concepts was also necessary.

The conclusion of this study also paves the way for new research project possibilities, involving the creation of new software for the FPGA-based processor, uploading this processor to other boards, creating other types of RISC-V architecture processors, and studying other microprocessor architectures.

In summary, this research project allowed for interaction with a field of study that is constantly evolving, which not only keeps up with but often sets the rules of the market. Finally, the coverage of hardware and software studies in this project allowed for a multidisciplinary study.

Acknowledgements

To the FEI University Center, for providing the opportunity and physical structure for the studies and Macnica DHW Brasil, for providing the FPGA DE1-SoC board.

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A Study on THD, SNR, and ENOB in Sigma-Delta Modulators

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1. Abstract

This study explores the sigma-delta modulators, focusing on their performance in terms of harmonics and noise metrics. We emphasize the critical role of oversampling and digital filtering in enhancing the resolution and minimizing harmonic distortions, which are vital for achieving precise analog-to-digital conversions in in space environments prone to radiation.

2. Introduction

In aerospace applications, choosing the right type of analog-to-digital converter (ADC) is pivotal for optimizing the performance and reliability of electronic systems in space missions [1]. Discrete-time ADCs are known for maintaining signal accuracy under radiation through specific mitigation techniques, whereas continuous-time ADCs provide advantages such as lower sensitivity to jitter and generally simpler circuit designs, which may reduce failures caused by radiation [2]. These factors highlight the critical need to weigh radiation tolerance, design simplicity, and system stability carefully in selecting ADCs for the demanding environment of space electronics [1,2].

Optimizing discrete-time sigma-delta (Σ-Δ) modulators in ADCs is essential for reducing Total Harmonic Distortion (THD) and enhancing Signal-to-Noise Ratio (SNR), utilizing precise capacitor charge-discharge cycles. Controlled by non-overlapping clock signals, this methodology effectively attenuates errors attributed to component mismatches and thermal variability, thus diminishing noise and harmonic distortion. Such optimization not only improves SNR but also minimizes THD, satisfying the demanding specifications of aerospace applications. [3].

This study highlights the importance of managing THD and SNR to maintain the integrity of digital signals, underscoring the need for design optimizations to enhance analog-to-digital conversion accuracy in radiation-sensitive applications.

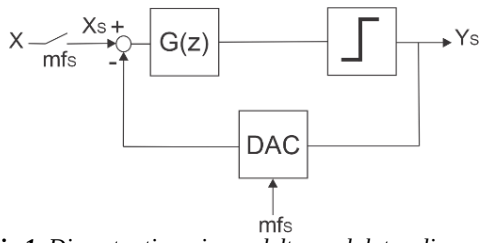

Fig.1. *Discrete- time sigma-delta modulator diagram.*

3. THD, ENOB and SNR

Studying noise and harmonic impacts is critical for optimizing Σ-Δ ADC performance, as they directly degrade signal accuracy and quality. We will next explore some of these key metrics.

The Effective Number of Bits (ENOB) is a metric for quantifying the resolution of an ADC. This parameter is given by:

$$ENOB = \frac{-10\log\left[10^{-SNR/10} + 10^{-THD/10}\right] - 1.76}{6.02}, \qquad (1)$$

where *SNR* represents the Signal-to-Noise Ratio, and *THD* is Total Harmonic Distortion. Lowering THD improves signal fidelity by minimizing harmonic distortions, leading to higher *ENOB*, thus enhancing resolution and accuracy in digital representation of analog signals.

The parameter *THD* is defined as:

$$THD = \frac{\sqrt{\sum_{k=2}^{\infty} V_k^{\,2}}}{V_1}, \qquad (2)$$

where V_k is the amplitude of the *k-th* harmonic and V_1 is the amplitude of the fundamental harmonic.

In the design of a Σ-Δ ADC, the *SNR* is given by:

$$SNR \approx 10\log\left[\frac{3}{2}\left(2^N - 1\right)^2 \cdot \left(\frac{2L+1}{\pi^{2L}}\right) \cdot M^{2L+1}\right], \qquad (3)$$

where *M* is the oversampling rate, *L* is the order of the modulator, and *N* is the number of bits in the quantizer resolution.

The selection of *M*, *N*, and *L* parameters is critical for optimizing the SNR of an ADC. A higher *M* allows the ADC to reduce noise outside the band of interest, thereby improving the effective SNR within the desired signal band. Additionally, a larger *N* in the quantizer enables better resolution, reducing quantization noise and contributing to a higher SNR. Lastly, the parameter *L* affects how noise is shaped in the frequency domain. Higher-order modulators tend to push more noise towards higher frequencies, which, when combined with oversampling, results in an improved SNR within the band of interest. Therefore, the design of a Σ-Δ ADC requires careful consideration of these parameters to achieve the best performance possible.

4. Results

Figure 2 shows the relationship between ENOB and THD for different SNR values. It indicates that an ADC designed for an 18-bit ENOB at -86.0 dB THD, and another designed for a 16-bit ENOB at -86.3 dB THD, both effectively degrade to the resolution of a 14-bit ENOB ADC at -100 dB THD. This demonstrates that high THD levels can significantly diminish the effective resolution of an ADC, regardless of its ideal ENOB specifications.

Figure 3 presents the correlation between the ENOB and THD for Σ-Δ ADC, with a clear indication that an elevated oversampling rate (*M*) improves ENOB. This is in line with the fundamental principles of the sampling theorem, suggesting that a higher *M* not only refines spectral resolution but also diminishes quantization noise, thus enhancing signal accuracy. An increased *L* further elevates ENOB by dispersing noise across an extended frequency spectrum, which is subsequently filtered. In the domain of harmonic distortion, a higher *M*, particularly in conjunction with suitable digital filtering techniques, can effectively mitigate harmonic distortion by allowing for finer resolution and reduced quantization noise.

The choice of modulator order in Σ-Δ ADC directly influencing signal quality in space applications. Second-order modulators are commonly used for their simplicity and robustness, but higher-order modulators, such as third or fourth order, offer better performance in suppressing noise in higher frequency bands, with a significant improvement in the SNR in environments with high levels of radiation.

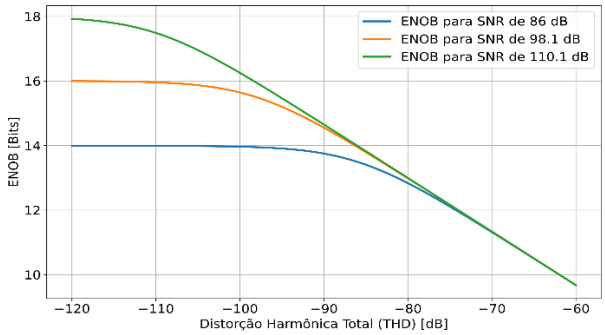

Fig.2. *THD versus ENOB for specific SNR values.*

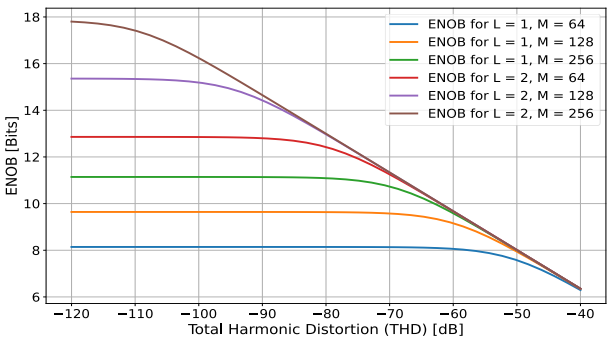

Fig.3. *THD versus ENOB for different N and M values.*

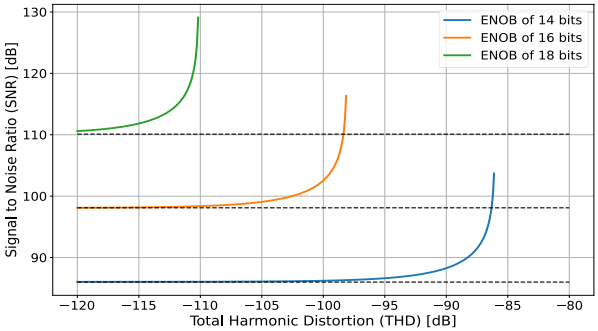

Fig.4. *THD versus SNR for Specific ENOB Values.*

Figure 4 illustrates the relationship between THD and SNR for specific ENOB values. Notice the importance of ensuring that the SNR maintains a margin relative to the THD. For an ADC with an ENOB of 16 bits, for example, the SNR should be 98.1 dB for a THD of -110 dB. For a THD of -98 dB, the SNR needs to be increased to 110 dB, ensuring that the overall system performance is not hampered by harmonic distortion and that the integrity of the digital output closely represents the original analog signal.

Again, it is crucial to ensure that harmonics do not compromise signal quality. Additionally, leveraging the benefits of a higher oversampling rate (*M*) not only improves the ENOB but also reduces harmonic distortion by enhancing spectral resolution and decreasing quantization noise, further ensuring the integrity and accuracy of the ADC's output.

5. Conclusions

The interplay among THD, SNR, and ENOB is crucial for optimizing ADC performance. Minimizing THD and maximizing SNR expands the effective dynamic range of the ADC, leading to a higher ENOB. Nonetheless, it's essential to recognize that an elevation in THD can compromise SNR, thereby constraining the effective resolution captured by ENOB.

Acknowledgments

This study was supported by the National Council for Scientific and Technological Development (CNPq), Brazil.

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Optimization and Fine-Tuning of AZ®P4620 Photoresist Parameters for Precision Coating

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1. Abstract

This article presents the results of a comprehensive study conducted at CTI Renato Archer, focusing on the optimization of spin-coating parameters and developer exposure for the AZ®P4620 photoresist [1], a key material in the photolithography process where it is used to create patterns on semiconductor wafers [2][3]. The thickness of the photoresist coating is crucial for the resolution and quality of the patterns, and inconsistencies in this thickness can lead to defects in the final device [4].

The motivation for this study came from the observation of inconsistencies in the thickness of AZ®P4620 photoresist using the default spinning program at the cleanroom facilities. These inconsistencies prompted the need for optimization of the spin-coating process [5]. The goal was to achieve a more controlled and consistent thickness of the photoresist coating, which would in turn improve the quality and reliability of the patterns created during photolithography.

To address this, three experiments were conducted. The first experiment investigated the impact of various factors on the thickness of the photoresist coating. These factors included the quantity of photoresist used, the parameters of the spin-coating process, and the temperature at which the process was carried out. The aim was to identify the optimal conditions for achieving a consistent and controlled thickness of the coating.

The second experiment focused on adjusting the lithography parameters for AZ®P4620 photoresist. The lithography process involves exposing the photoresist coating to UV light using the MicroWriter ML®3 [6] via direct-write lithography using a software mask, which creates the desired pattern on the coating. The parameters of this process, such as the dose of UV light and the focus correction, can significantly affect the quality of the resulting structures. The aim of this experiment was to identify the optimal lithography parameters for AZ®P4620 photoresist.

The third experiment characterized the development time for photolithography with AZ®P4620 photoresist. The development process involves immersing the exposed photoresist coating in a solution of AZ®400K developer [7], which removes the parts of the coating that were exposed to UV light, revealing the pattern. The quantity of developer used, the development time, and the temperature at which the process is carried out can all affect the quality of the resulting structures. The aim of this experiment was to identify the optimal conditions for the development process.

The results from the first experiment revealed that the average thickness of the coating decreases with an increase in initial photoresist quantity. This was a counterintuitive result, as one might expect that using more photoresist would result in a thicker coating. However, the results showed that this was not the case. Additionally, it was found that including a spread time in the spinning program marginally improved the uniformity of the coating. The initial temperature of the resist at the time of application was also found to have a minimal effect on the resulting thickness of the coating.

The second experiment showed that a UV dose of 200 mJ/cm² is the lower limit for complete photoresist sensitization. This means that a dose of 200 mJ/cm² is the minimum amount of UV light required to fully expose the photoresist. It was also found that a focus correction within -2µm to +2µm provided satisfactory resolution of the resulting structures. The third experiment indicated that a lower quantity of fresh developer solution at 23ºC for 5 minutes was optimal for the development process. It was also found that reusability of the developer solution in small batches is possible.

These findings contribute significantly to the goal of improving the reproducibility of micro- and nano-scale structures fabrication, offering insights into the optimization of photolithography processes in the cleanroom facilities at CTI Renato Archer. Despite these advancements, the study still identified some reproducibility issues when fabricating very complex designs at lower scales, suggesting the need for further research. It is recommended additional experiments to investigate the contrast curve of the photoresist.

2. Conclusions

The study successfully optimized the spin-coating parameters and developer exposure for AZ®P4620 photoresist. The key findings include the optimal lithography parameters for a 7000 rpm spin-coated layer with an average thickness of 5.5μm, which are a UV dose of 250 mJ/cm² and a focus correction of 0μm. Additionally, the ideal quantity of AZ®400K developer for a 2-inch silicon wafer is 25mL, used for 5 minutes at 23ºC. This emphasizes the importance of using fresh developer and gentle agitation to ensure even development.

Despite these advancements, the study identified reproducibility issues when fabricating complex designs at lower scales, suggesting the need for further research. It recommends additional experiments to investigate the contrast curve of the photoresist. The findings contribute to the broader understanding of microfabrication processes and underscore the necessity for ongoing experimentation to refine photolithography techniques for micro- and nano-scale structures.

Acknowledgments

The author extends heartfelt gratitude for the financial support received from CNPq under process #301604/2023-1, which was instrumental in the completion of this research. Additionally, the research was conducted under PRJ 02.112 within the Assembly, Packaging & Systems Integration Division – DIMES at CTI Renato Archer. The contributions and support provided by these entities were invaluable to the resolution of this study.

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Analysis of the Influence of Mechanical Stress on SOI FinFETs in a Transconductance Operational Circuit

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1. Abstract

This study investigates the effect of uniaxial mechanical stress applied to triple-gate SOI FinFET devices. The main basic parameters of the devices are evaluated, demonstrating the improvement achieved by strained devices compared to unstrained one. For a more thorough analysis, the devices were employed in a transconductance operational circuit, showing that the circuit designed with strained devices exhibited better performance compared to the circuit designed with unstrained devices.

2. Introduction

Various studies have explored advancements in electronic devices towards smaller and more efficient designs. As devices shrink in size, they encounter the short-channel effect, leading to degradation of specific parameters and ultimately compromising performance [1]. With the decrease in device size triggering short-channel effects, research has delved into novel approaches to address or mitigate this issue.

New devices have emerged, among them the Triple-Gate FinFET. Due to its structure, it possesses good electrostatic coupling, leading to enhanced performance and enabling operation at the nanoscale [**Erro! Fonte de referência não encontrada.**].

Given that high-performing devices require thin and tall fins, most carriers tend to flow through the sidewalls, which exhibit lower electron mobility compared to the top of the transistor due to crystal orientation [2]. Accordingly, to address this issue and enhance carrier mobility, thereby increasing current capacity, the method of mechanical channel strained was employed [3]. This technique applied to the device with the aim of augmenting carrier mobility, leading to a notable rise in drain current, thus rendering it more efficient compared to strained devices [4]. Mechanical stress can be categorized based on its direction of application: uniaxial, applied solely along the channel length, or biaxial, applied in two directions [5].

For this work, the mechanical stress applied to all devices was of the uniaxial type, as it is more efficient for smaller devices [6]. A transconductance operational circuit was designed to test the performance of these strainde and unstrained devices, for a comparative analysis.

3. Devices characteristics and circuit

In this study, FinFETs with physical attributes were employed a channel length (L)150nm, fin height (H_{FIN}) of 65nm, a fin width (W_{FIN}) of 20nm, and an effective width (Weff) of 150nm, all devices comprise 5 fins. Fabrication occurred at Imec, Belgium, with additional process details provided in the source [7]. The structure of the device is depicted in Figure 1.

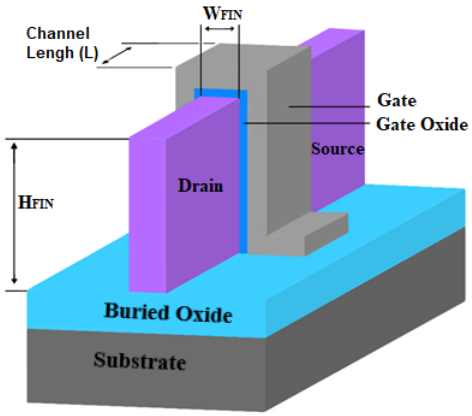

***Fig. 1** - Device Structure [8]*

The Figure 2 depicts the circuit designed for this work, where devices M8, M5, and M7 form the current mirror. Devices M1, MS, M3, and M4 constitute the first-stage differential pair, while device M6 forms a common-source amplifier for the second stage. The capacitors CC and CL represent, respectively, the compensation capacitor (60fF) and the circuit load (200fF).

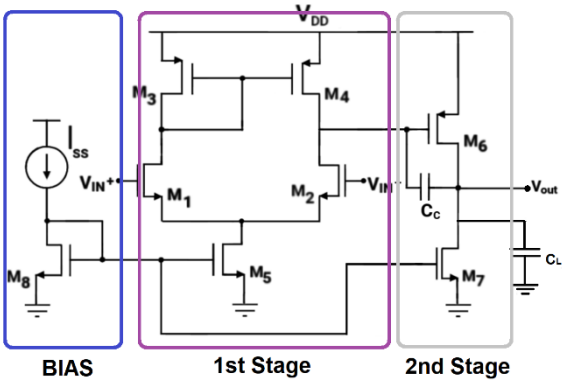

***Fig. 2** - Designed Circuit*

4. Results and discussion

The first analysis conducted focused on the basic parameters of the device. Regarding drain current, mechanical stress increases the carries mobility increasing the drain current and consequently increases transconductance as well. Another observation regarding uniaxial mechanical stress is that it showed to be more efficient in n-type devices than in p-type devices. The variation of threshold voltage was negligible the last analyzed parameter was the Early Voltage, which also presents a better response for strained devices.

The Figure 3 shows the Phase Margin in relation to the Gain Ad of the circuit. Was observed circuits are stable, with a phase margin of around 60°, and that the circuit designed with strained devices exhibits higher gain compared to the circuit designed with unstrained devices

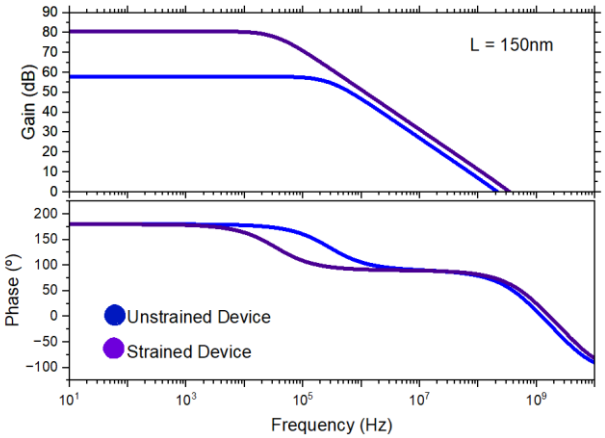

***Fig 3** - Phase Margin and Gain*

Table 1 shows the main results of the analysis of the circuit designed with unstrained and strained devices.

***Table 1** – Main Results*

Parameters	Unstrained	Strained
Phase (º)	67	63
GBW (MHz)	214	345
Gain (dB)	58	81
Power (µW)	171	221
Iss (µA)	28	38

Through the results, it is evident that mechanical stress proves to be a highly effective technique. The circuit designed with strained devices exhibited a significantly higher GBW, achieved a higher voltage gain, and remained stable with a phase margin of 63°. Analyzing power dissipation, the circuit designed with strained devices shows higher dissipation, attributed to the straining increasing the current and consequently resulting in higher power.

Conclusions

With these results, it is possible to conclude the benefits brought by mechanical stress. In relation to the device, it manages to enhance the main basic parameters of the devices such as drain current, threshold voltage, subthreshold slope, transconductance, and Early voltage. By applying strained devices in a two-stage transconductance operational circuit, the devices were able to provide good performance, exhibiting higher GBW and voltage gain compared to the circuit designed with unstrained devices, albeit at the expense of power dissipation.

Acknowledgments

The authors would like to thank CAPES, CNPq and FAPESP for the financial support and Imec for providing the samples used in this work.

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