Back Gate Bias Influence on Threshold Voltage at pMOS and nMOS SOI Ω-gate Nanowire down to 10nm Width

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1. Abstract

This paper shows the influence of back gate bias on threshold voltage for nMOS and pMOS SOI Ω-gate nanowire, for a different width. Wider devices present more influence of back gate bias while for narrow devices it can be neglected for many applications.

2. Introduction

Due to technological evolution, the challenge of reducing the scaling of devices becomes ever more difficult. The Silicon-On-Insulator (SOI) technology is an alternative to reduce the dimensions of the transistors. Different geometries are also studied in order to increase the density of transistors in an integrated circuit. The nanowire (NW) gate-all-around (GAA) transistors are one of the main devices studied by the scientific community.

The aspect that draws most attention to GAA structure is the possibility of maximize the electrostatic gate control, however, this structure demands a high level of complexity in manufacturing. The SOI Ω-gate nanowire, on the other hand, has a reduced manufacturing complexity and keep the electrostatic confinement [1-4]. Different studied are already done in this NW devices, in [5-9] the performance of NW with respect to strain on mobility was studied, low-frequency noise in [10, 11], crystallographic orientation [7, 10, 11], and scalability effects [1, 5, 12] are also studied. The initial study of back gate bias was done in [13] for nMOS SOI Ω-gate nanowire. And in this paper, the influence of back gate bias on threshold voltage for nMOS and pMOS SOI Ω-gate nanowire will be analysed.

3. Devices Characteristics

The SOI Ω-Gate NW transistors studied in this paper were fabricated at CEA-LETI. They have a 145 nm of buried oxide thickness on (100) SOI wafers. The gate stack is composed by HfSiON/TiN (EOT=1.3nm) and the silicon height (H_{NW}) is 11 nm. More details about the fabrication of these devices can be obtained in [1].

The devices studied have the width (W_{NW}) ranging from 220nm down to 10 nm and the channel length is 100 nm. This channel length was chosen in order to analyse the back gate bias influence without the influence of short channel effect (SCE)

Figure 1 shows the SEM and cross sectional TEM images of the device [1]. There is only one difference comparing the conventional trigate and this device, which is the H_2 anneal used to round the NW [1].

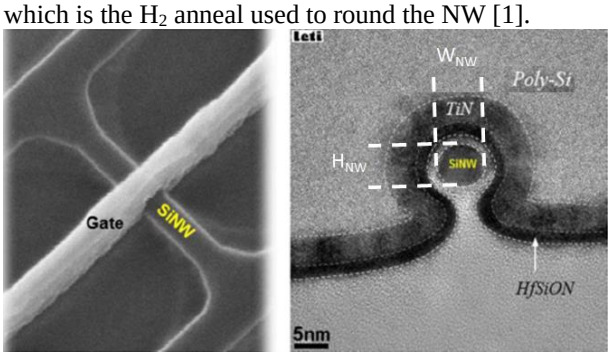

***Fig 1** - (Left) SEM and (right) cross-sectional TEM images of SOI Omega-Gate Nanowire [1].*

4. Results and Analysis

Figure 2 shows the normalized drain current as function of front gate bias (V_{GS}) to different back gate bias (V_B) (from -20V to 20V) of pMOS (A) and nMOS (B) Ω-Gate NW for narrow device (W_{NW}=10nm).

It is possible to see for narrow devices that the variation of back gate bias does not significantly influence on drain current. This occurs because when the channel is narrow the electrostatic gate control is maximized and the Ω-Gate device approaches a GAA device.

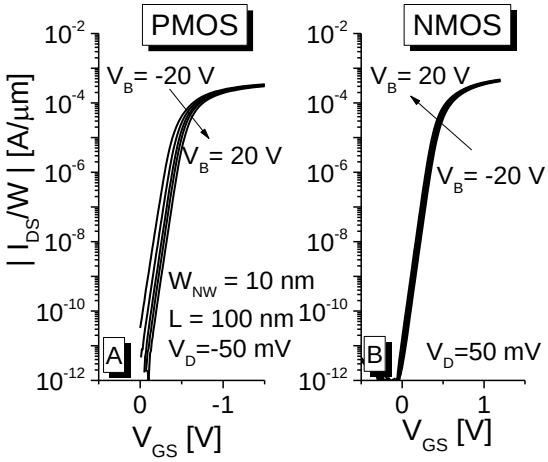

***Fig 2** - Normalized by W_{NW} drain current of Ω-Gate NW for width of 10 nm on pMOS device (A) and nMOS (B) for different back gate bias (V_B).*

On the other hand, figure 3 shows the normalized drain current as function of front gate bias to different back gate bias (from -20V to 20V) of pMOS (A) and nMOS (B) Ω-Gate NW for wider (220nm) width.

This figure shows that in wider devices the variation of back gate bias influence directly in drain current, consequently, in the threshold voltage. These wider devices have lower electrostatic gate control, once the wider devices is a quasi-planar UTB SOI MOSFETs [13]

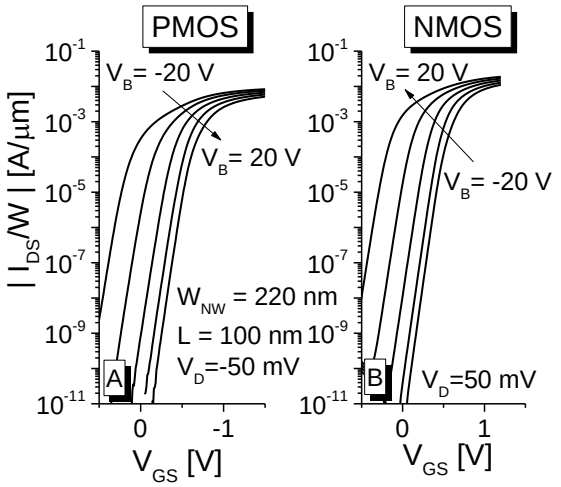

Fig 3 *– Normalized by W_{NW} drain current of Ω-Gate NW for width of 220 nm in pMOS device(A) and nMOS (B) for different back gate bias (V_B).*

Figures 4 and 5 show, respectively pMOS and nMOS, threshold voltage as function of back gate bias for different channel width.

It is possible to see, that as the channel narrows, the dependence of back gate bias decreases. Devices with 10 nm of width has slightly variation on threshold voltage for pMOS and nMOS when the back gate changes. Devices with 220 nm of width has a large variation on threshold voltage in the range studied.

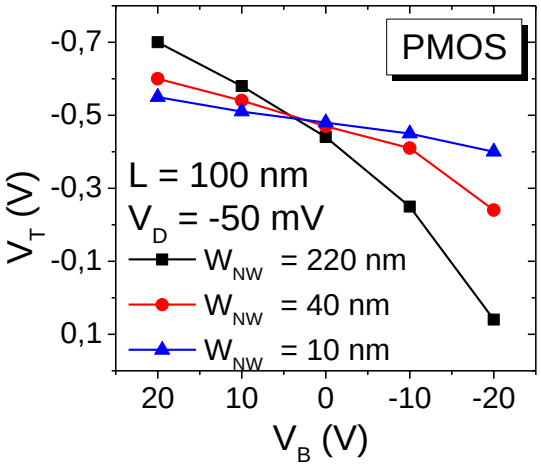

Fig 4 *- Threshold voltage as a function of back gate bias for different channels widths on pMOS devices*

When the back interface tends to inversion mode (more negative for pMOS and more positive for nMOS) the threshold voltage tends to zero, once the channel is already inverted. This behaviour is presented in figures 4 and 5.

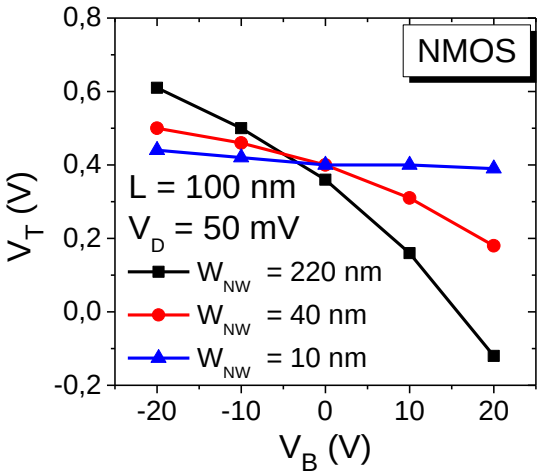

Fig 5 *- Threshold voltage as a function of back gate bias for different channels widths on nMOS devices.*

5. Conclusions

This work presents an analysis of back gate bias influence on threshold voltage for pMOS and nMOS SOI Ω-gate nanowire. In a range of +20V and -20V the threshold voltage variation for wider devices (220 nm) reached 800 mV, while for narrow devices (10 nm) this variation is not more than 150 mV, and can be neglected for many applications.

Acknowledgments

The authors acknowledge CNPq, CAPES, FAPESP for financial support.

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