Influence of the dimensions on pFinFET devices towards the self-heating effect

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1. Abstract

This paper presents the results of an experimental electrical analysis of the self-heating effect on p-type trigate FinFET transistors as their dimensions are varied.

2. Introduction

Since the introduction of the Semiconductor-On-Insulator (SOI) technology, the self-heating effect (SHE) has become a concern to the industry. Although the buried oxide presents a series of advantages to the electrical characteristics of the devices, it makes the evacuation of the heat generated in the device's channel due to the current flow more difficult, increasing significantly the temperature [1].

The main consequence of the temperature increase in a MOS transistor is the decrease in its drain current, due to carrier mobility degradation. It is modelled according to (1):

$$\mu_{eff} = \mu_{eff,0}(T/T_0)^{-k} \quad (1)$$

Where μ_{eff} is the effective mobility at temperature T, $\mu_{eff,0}$ is the effective mobility at temperature T_0 and k is the mobility temperature coefficient [2].

Newer technologies, such as the ultra-thin body and buried oxide (UTBB) and the FinFET have improved the thermal characteristics, respectively reducing the buried insulator's length and increasing the device's surface area with the three dimensional body, which results in lower thermal resistances, and therefore presenting a weaker temperature increase than conventional SOI devices at the same power conditions [3].

However, small enough devices may still present significant SHE, even when the aforementioned technologies are employed, since they have less surface area to dissipate the heat generated [4]. Reference [5] presents an example of a pFinFET, which suffers SHE, evidenced by its negative output conductance (g_{DS}) [6]. Thus, further investigation must be conducted in order to determine the importance of this effect in current technologies.

3. Devices Characteristics

The triple-gate pFinFET devices here studied were fabricated in imec on (100) SOI substrates, with a buried oxide 150nm thick, gate composed of a 100nm polysilicon layer over 5nm TiN, fin height (h_{fin}) of 65nm, channel presenting the natural wafer doping (N_a=1x10^{15} cm^{-3}), gate dielectric of 2nm HfO_2 and 1nm SiO_2 (EOT = 2nm). All devices have five fins in parallel and multiple channel lengths (L) and fin widths (W_{fin}). Fig. 1 presents the basic structure of the FinFET transistors, with its main dimensional characteristics.

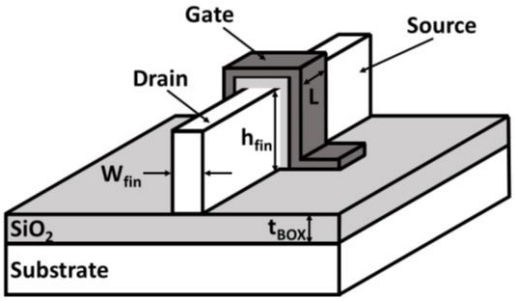

Fig.1. *SOI FinFET*

4. Analysis and Results

A first approach to observe the existence of the SHE is through the g_{DS} of a saturated device. Fig. 2 presents the normalized drain current (I_{DS}) of the pFinFET for multiple long channel devices (L=1µm) with different widths as a function of the drain voltage (V_{DS}). In addition, the inset of this figure presents the g_{DS} of those devices in the saturation regime. Similarly, Fig. 3 presents the same curves, but for devices with shorter channels (L=130nm).

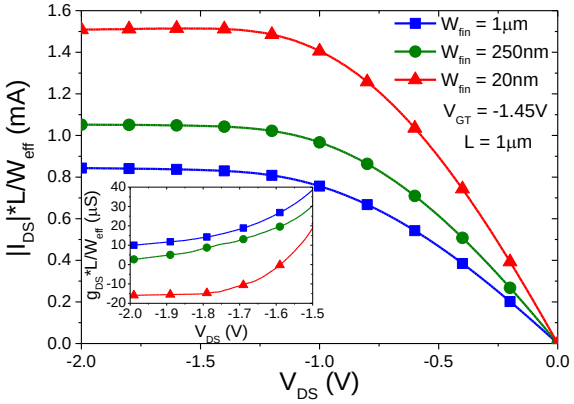

Fig.2. *Normalized drain current as a function of the drain voltage varying the fin width for a channel length of 1µm*

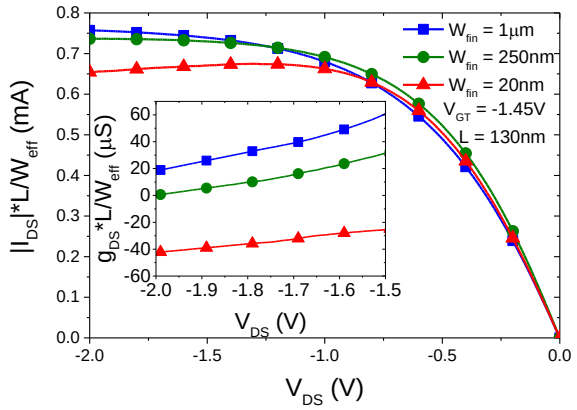

Fig.3. *Normalized drain current as a function of the drain voltage varying the fin width for a channel length of 130nm*

Since the sidewalls of the FinFET are not on the same plane as the top layer, they should present different mobilities. Thus, μ_{eff} is calculated as shown in (2):

$$\mu_{eff} = (\mu_{top}W_{fin}+\mu_{lat}2h_{fin})/(W_{fin}+2h_{fin}) \quad (2)$$

This equation is a weighted average of the top (μ_{top}) and lateral (μ_{lat}) mobilities, using W_{fin} and $2h_{fin}$ respectively as weights [7]. As a result, μ_{eff} is a function of W_{fin}, as presented in Fig. 4.

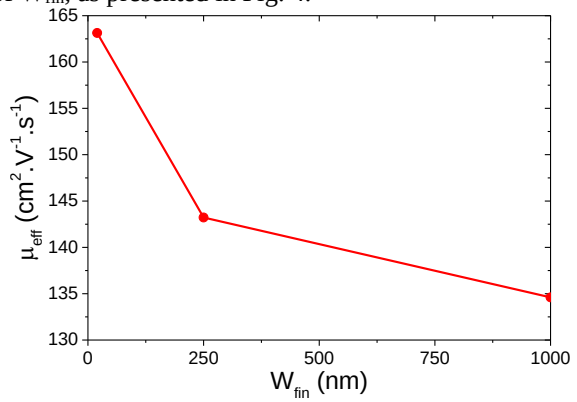

Fig.4. *Calculated mobility as a function of the fin width*

In order to obtain the graph of Fig. 4, μ_{top} and μ_{lat} were extracted from devices with long channels (L=1µm) and two different fin widths: one narrow (W_{fin}=20nm), to approach the value of μ_{lat}, and one wide (W_{fin}=1µm), to approach the value of μ_{top}. The Y-function method was employed to avoid the series resistance problem.

Since the normalization in Fig. 2 and Fig. 3 does not account for the difference in μ_{eff}, the narrower fins should present higher current levels, as expected from Fig. 4. In addition, devices with narrower fins should present even larger normalized currents due to the stronger coupling between gates, resulting in a better control of the charges in the channel. Although Fig. 2 meets those expectations, the same does not happen for Fig. 3, where $I_{DS}(W_{fin}$=20nm) is below $I_{DS}(W_{fin}$=250nm) even for V_{DS} values close to zero, and eventually reaches levels below $I_{DS}(W_{fin}$=1µm) at lower V_{DS}.

Considering the negative trend for g_{DS} as V_{DS} is lowered, and that the only difference between Fig. 2 and Fig. 3 is the channel length, an explanation for the lower normalized current levels for smaller devices is the SHE. As the dimensions are reduced, there is a decrease in the total surface area available to dissipate the heat generated. Particularly, for the case where L=130nm and W_{fin}=20nm (that is, the device with smallest surface area), the effect is strong enough to degrade the current at lower power levels, and to degrade g_{DS} to more negative values further in the saturation region.

Due to the channel modulation effect, it is not possible to establish an immediate numerical relation between the DC measured g_{DS} and the SHE; however, a first order comparison among devices with the same channel length seems to yield results that confirm the presence of this effect in the studied transistors, and its association with the devices' dimensions.

5. Conclusions

The relation between SHE and p-FinFET devices dimensions was experimentally assessed in this work, stressing the connection between surface area and total thermal resistance of the device, additionally confirming the relevance of this effect for FinFET technology at smaller dimensions.

Acknowledgments

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