Ring Oscillators: Comparative Approach for SET Tolerant Structures

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1. Abstract

This work summarizes the results from a comparison involving 3 architecture-based strategies for Single Event Transients SET robustness implementation in voltage controlled ring oscillators VCRO. The results indicate that, considering a common delay cell, rising levels of noise performance and SET robustness are obtained in multi coupled structures at the cost of area and power, for the same tuning sensitivity.

2. Introduction

Voltage controlled ring oscillators VCRO [1] has been widely applied in multiple applications involving the frequency synthesis for control, instrumentation, and telecommunication systems design. On the other hand, the reduction of technology nodes, the decreased levels of power consumption and the requirements for high frequency operation create limits in applications for aerospace environments, considering the presence of ionizing radiation induced effects. Implemented at device, topology or architecture level, design-based mitigation techniques involve the application of space redundancy structures and establish a trade-off between the level of robustness and the area and power consumption.

In this context, by applying a proposed evaluation metric, this work establishes a performance comparison considering 3 coupled rings-based architectures of voltage controlled ring oscillators VCRO for system level SET robustness implementation [2].

2. Ring Oscillators: Implementation Features

The proposed architecture-based performance comparison considers 3 reference structures for delay cell interconnection. The first architecture A_1 is a standard 3-stage based single-path ring (Fig. 1), the second architecture A_2 applies the first one for composing 2 coupled rings (Fig. 2), and the third one A_3 applies the same coupling pattern in a triple ring (Fig. 3). A reference topology for delay cell was adopted considering a self-biased fully-differential-based structure with 2 complementary cross-coupled pairs (NMOS and PMOS), according to the Fig. 4(a). Thus, considering a common delay cell applied in different coupling levels from a common ring structure, the same characterization data for the tuning sensitivity (F_{OUT} x V_C) is obtained, according to the Fig. 4(b).

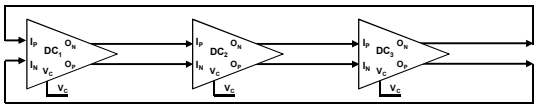

Fig.1. *Architecture 1 (A_1): single path ring with 3 delay cells.*

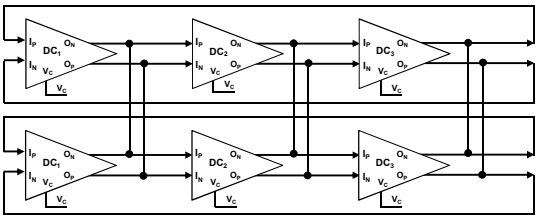

Fig.2. *Architecture 2 (A_2): 2 coupled rings (6 delay cells).*

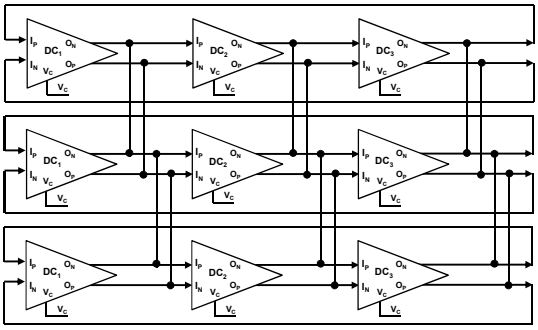

Fig.3. *Architecture 3 (A_3): 3 coupled rings (9 delay cells).*

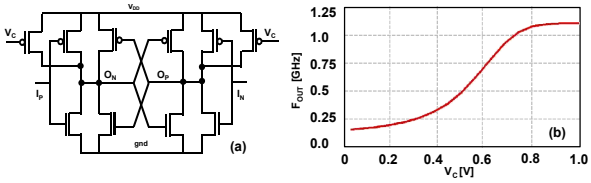

Fig.4. *VCRO: (a) delay cell topology, (b) tuning sensitivity.*

3. Results

From schematic level implementation, the VCRO-based circuits were designed at Cadence Analog Design Environment ADE by applying CMOS technology (UMC L180). The adopted simulation conditions consider a set of common operating features: power supply V_{DD} = 1.2 V, total current consumption for delay cell I_{DC} = 82 µA, and operating frequency Freq = 900 MHz. Additionally, the SET emulation at simulation environment was obtained through a current pulse with upper value I_{MAX} = 1.5 mA, and pulse length in time scale Δt_P = 500 ps [3][4][5][6]. The circuit sensitivity to SET current pulse is evaluated considering the resulting

output signal phase displacement ΔΦ. Derived from a standard Figure of Merit FoM_1 [7] for describing the noise/consumption-based trade-off in oscillators, a complementary Figure of Merit FoM_2 is proposed in this work for a general performance evaluation (considering ΔΦ as an additional parameter to the previous model), according to (1).

$$FoM_2 = 10\log\left(\frac{P_{DC}}{1mW}\right) + L(\Delta f) - 20\log\left(\frac{f_0}{\Delta f}\right) + 20\log(\Delta\Phi) \quad (1)$$

Thus, Fig. 5 illustrates the phase noise PN@Δf characterization obtained for each architecture (A_1 in red line, A_2 in blue line, and A3 in green line) considering an offset frequency range Δf = 3 MHz. Additionally, from transient analysis, Fig. 6 presents a comparative overview about the SET induced phase displacement ΔΦ for each structure, illustrating the output waveform without distortion (Fig. 6(a)(b)(c) in black), SET induced distortion and $\Delta\Phi_1$ in architecture A_1 (Fig. 6(a) in red), $\Delta\Phi_2$ in A_2 (Fig. 6(b) in blue), and $\Delta\Phi_3$ in A_3 (Fig. 6(c) in green). Each distorted waveform is associated with a corresponding time scale displacement data Δt. Considering the indicated curves, Table I summarizes a numerical characterization for the set of reference performance parameters (power consumption P_{DC}, phase noise PN@Δf, and phase displacement ΔΦ), and a final numerical evaluation by applying the standard Figure of Merit FoM_1, and the proposed Figure of Merit FoM_2.

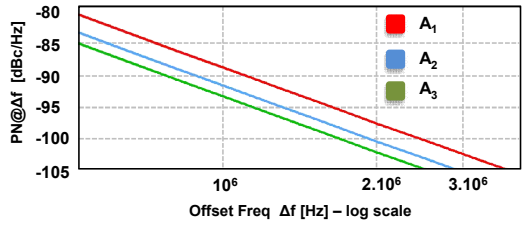

Fig.5. *Phase Noise PN: Freq = 900 MHz, Δf = 1MHz.*

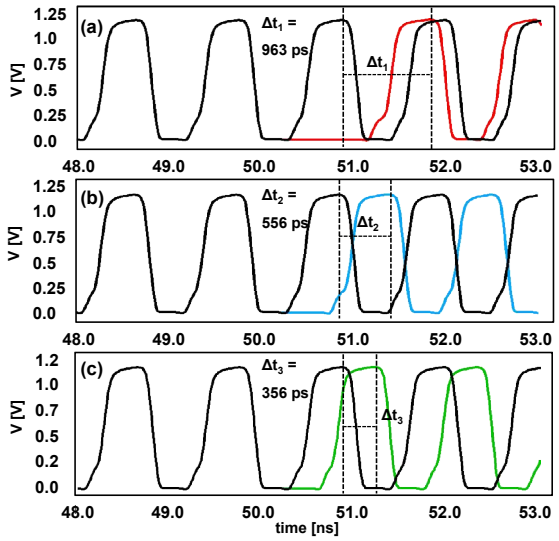

Fig.6. *SET effects (VCRO architectures): (a) A_1, (b) A_2, (c) A_3.*

Table I. *VCRO architectures: performance comparison*

Performance Parameters	VCRO Architecture		
	A1	A2	A3
Delay cells N	3	6	9
Power Consumption P_{DC} [mW]	0.392	0.783	1.175
Phase Noise PN@1MHz [dBc/Hz]	-88.9	-91.8	-93.5
Phase Displacement Φ [degrees]	312	180	115.3
Standard FoM (FoM_1)	-235	-231	-228.9
Proposed FoM (FoM_2)	-120	-127	-134

4. Conclusions

This paper described a comparative evaluation involving 3 architectural variants for VCRO, with a common structure for delay cell. From the performance comparison, the results indicate that rising levels of coupling for ring-based structures imply on a rising phase noise PN@Δf performance and SET robustness, considering a proportional cost in area, power consumption and input capacitance. Thus, the verified operating features from A_1 to A_3 involve a linear increase in P_{DC}, a approximated linear decrease in PN@Δf and a nonlinear decrease in ΔΦ. Considering a FoM-based evaluation, as related in the Table I, A_1 demonstrates the higher level of performance according to FoM_1 and, on the other hand, considering the operation with SET robustness, A_3 demonstrates a higher general performance, according to FoM_2.

Acknowledgments

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