Simulation Analysis of Fin Width Influence in Junctionless MOSFET Effective Mobility: from Quasi-Planar to Nanowires

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1. Abstract

Junctionless effective mobility was studied for several fin width ranging from quasi-planar to nanowire devices. The results show that with decreasing Coulomb scattering, smaller fin width presents an improvement on the mobility.

2. Junctionless

Junctionless devices [1] have shown great potential for future nodes of integrated circuit. The absence of junctions reduce fabrication process steps, compared to the fabrication of sharp junctions for small inversion mode transistors [2-3]. Moreover, in electrical performance it shows great results with similar current drive while suppressing short channel effects [4]. Fig. 1 shows the junctionless device with its main parameters and the cross-section of this device.

The effective mobility of these devices is fundamentally different from the inversion device, since it has different conduction mechanisms. Junctionless transistor has its conduction at the interior of the silicon layer for low gate voltage represented by the bulk mobility while the gate voltage is smaller than the flat band voltage. For higher gate voltages, the conduction on the interfaces becomes more important, where the interface quality becomes relevant. Although there are several benefits of these devices, due to the high doping of the channel it's expect to have a great degradation due to ionized impurities scattering [3] which is the main scattering mechanism on these devices [5].

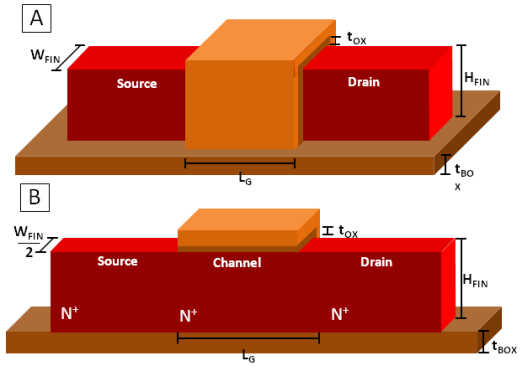

Fig.1. *(A) Junctionless transistor and (B) Cross section of a Junctionless device where W_{FIN} is the fin width, H_{FIN} is the fin height, L_G is the channel length, t_{OX} is the oxide thickness and t_{BOX} is the box thickness.*

3. Simulation

The n-type devices simulated were tridimensional structures on SOI substrate with buried oxide of 150nm, fin height (H_{fin}) of 9nm, channel length of 10µm and variable channel width, from quasi-planar with fin width (W_{fin}) of 10µm to nanowire of 30nm. The equivalent oxide thickness is 1.3nm and the devices possess metal gate with mid gap material (Φ_M=4.7eV) followed by polysilicon. These devices have drain extensions of 30nm. The doping of these devices is 5.10^{18} cm^{-3} with Arsenic. For these simulations, the models used were Generation-Recombination with doping dependence, bandgap narrowing and the carrier mobility described by the model of [6], which accounts for the mobility in the accumulation layer.

4. Mobility Extraction

For the extraction of the mobility, the split-CV method was used, where with a curve of the capacitance of the gate-to-channel and the drain current as a function of the gate voltage, it can be extracted the effective mobility of these transistor by (1) and the carrier density by (2).

$$\mu_{eff} = \frac{L_G^{\,2} I_{DS}}{V_{DS} \int_{-\infty}^{V_{GS}} C_{GC}(V_{GS}) dV_{GS}} \tag{1}$$

$$N_{INV} = \frac{1}{L_G W_{eff} q} \int_{-\infty}^{V_{GS}} C_{GC}(V_{GS}) dV_{GS} \tag{2}$$

Where μ_{eff} is the effective mobility, I_{DS} is the drain current, V_{DS} is the drain voltage, V_{GS} is the gate voltage, C_{GC} is the capacitance of the gate-to-channel per unit area, W_{eff}= W_{fin} +2H_{fin}, and L_G is the channel length.

4. Results

For these simulations in the first case, the bulk mobility was first specified equally for both the top and the sidewalls of the channel and then the sidewalls for half of the top mobility for the second case, which represents smaller Coulomb scattering for the first case compared to the second one.

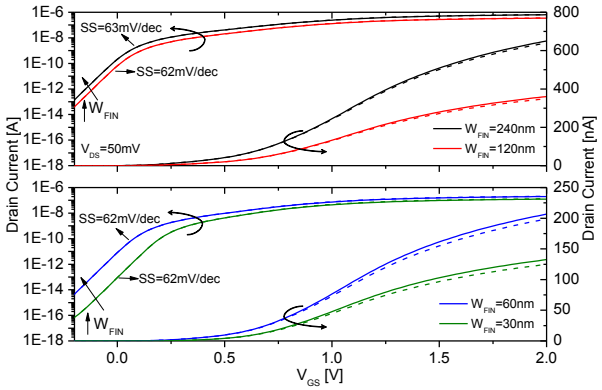

Fig.2. *Drain current as a function of the gate voltage for fin width from 30nm to 240nm. For solid line the top mobility equal the sidewalls and for dashed line the sidewalls mobility equals half of the top mobility.*

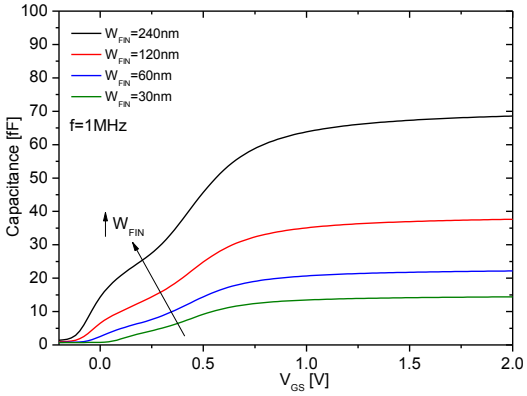

Fig.3. *Gate-to-channel capacitance as a function of the gate voltage for fin width from 30nm to 240nm.*

Fig. 2 shows the drain current of the devices as a function of the gate voltage with V_{DS}=50mV. Nearly ideal subthreshold swing (SS) can be seen for all devices and the threshold voltage decreasing with increasing fin width. Long channel length of the device made it possible to neglect the series resistance.

The gate-to-channel capacitance is shown in Fig. 3 we can see that the maximum capacitance vary with the W_{fin} and thus with the area of the device, similar to all cases. All devices have similar flatband voltage but shows reduced threshold voltage as the W_{FIN} increases.

With the method described in the previous section the effective mobility of these devices was extracted. Fig. 4 shows the effective mobility for several fin width as a function of the gate voltage. The results show that for both cases the mobility for the bulk conduction is higher for the larger fin width. As the device goes into accumulation, in the first case, the maximum mobility shows higher value for smaller fin width and in the second case for larger fin width.

These curves show that the maximum mobility has a slight increase as the fin width decreases in the first case. This has been reported in several papers experimentally [5,7]. The junctionless devices has a mobility increase with decreasing fin width mainly because of the reduced impurity scattering.

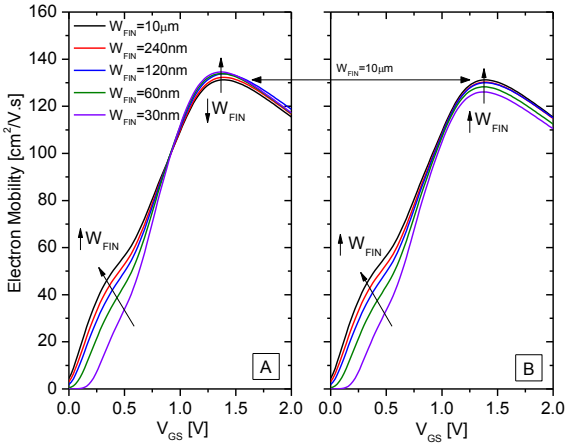

Fig.4. *Effective mobility as a function of gate voltage for fin width from 30nm to 10μm. For (A) the top mobility equals the sidewalls and (B) the sidewalls mobility equal half of the top.*

The reduction of the Coulomb scattering on these transistors increase the bulk mobility, as a sharper increase on the mobility for smaller gate voltage variation can be seen especially in small fin width. Which makes these devices show higher maximum mobility [5] as shown in the first case whereas in the second case the mobility has the opposite tendency as the Coulomb scattering increases.

5. Conclusions

This work studied the mobility behavior of junctionless devices as a function of fin width. Smaller fin width shows an improvement on the mobility as the device goes from quasi-planar to nanowire. The reduction of Coulomb scattering is the main cause of this carrier mobility improvement as the devices becomes narrower.

Acknowledgments

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