Analysis of Thermal Resistance with BOX Thinning in UTB SOI MOSFETs

F. J. Costa[1], R. Trevisoli[1] and R. T. Doria[1]
[1] Electrical Engineering Department, Centro Universitário FEI, São Bernardo do Campo, Brazil
e-mail: fernandoteccenter@hotmail.com

1. Abstract

This work discusses the behaviour of the thermal resistance with the thinning of the BOX in advanced Ultra-Thin Body SOI MOSFETs through 2D numeric simulations. SOI MOSFETs suffer from self-heating effect that degrades the output characteristics of the device, such that the thermal properties must be considered in the design of integrated circuits. Through this work, it could be observed that the buried oxide thinning has induced a nearly linear reduction in the thermal resistance, which becomes slightly steeper for thinner buried oxide thicknesses.

Keywords- SOI, Self-Heating, UTB, Thermal Resistance.

2. Introduction

The miniaturization of MOS device dimensions came up with the undesirable influence of the source/drain junctions on the channel charges, degrading their output characteristics [1]. These effects are so-called Short Channel Effects (SCEs) [2]. Aiming at reducing SCEs, the SOI technology (Silicon-on-Insulator) became an alternative to continue the miniaturization process with reduced undesirable effects [2]. This technology consists in the addition of an insulating layer between the substrate and the active region, where the devices are fabricated. The insulator, usually SiO_2, has worse thermal conductivity than silicon, making the device more susceptible to self-heating effect (SHE). As the carriers flow through the channel of the transistor, the lattice temperature increases, provoking the electron mobility reduction which leads to the degradation of its output characteristics.

Along the last years, several improvements have been proposed to SOI devices, such as the thinning of the active silicon layer, leading to the development of Ultra-Thin Body MOSFETs (UTB) [4]. The reduction on the silicon layer thickness (t_{Si}) induces a better capacitive coupling of the structure, reducing SCEs. However, this technology has the penalty of degrading the thermal conductivity of the devices, due to the smaller silicon area. More recently, a new SOI generation, so-called UTBB, has demonstrated the fabrication of devices with both reduced t_{Si} and buried silicon oxide layers (t_{box}). This technology enables the application of active substrate bias, i.e. the substrate can work as a second gate, improving the device performance and making it a strong candidate for low power applications with performance similar to multi-gate transistors [3]. It has been recently shown that the t_{box} reduction has led to a better thermal dissipation, reducing SHE [4]. For that reason, this work aims at evaluating the thermal behavior of UTB devices through the reduction of t_{box}, through the analysis of the thermal resistance of the devices by applying the hot chuck method [5].

3. Devices Characteristics

The simulated devices present gate length (L) of 25 nm, t_{Si} = 7 nm and gate oxide thickness of 2 nm. The buried oxide thickness has been varied between10, 20, 40, 60, 80, 100, 200 and 400 nm. The simulated devices present structures similar to the ones from [6] and have p-type ground plane with doping concentration of $1x10^{18}$ cm^{-3}. All the simulations have been performed using Sentaurus TCAD [7] and models accounting for the mobility dependence on vertical and longitudinal electric fields, bandgap narrowing have been considered. For taking into account the self-heating effect, the hydrodynamic has been used, which also considers the impact ionization effect in the output characteristics. The simulations have been calibrated according to the experimental results presented in [5] and [6]. Fig. 1 shows the simulated drain current (I_{DS}) as a function of the gate voltage (V_{GS}) for a high drain bias (V_{DS} = 1 V), indicating the influence of the self-heating effect on the device behaviour. It can be noted that when SHE is considered, there is a reduction in the drain current due to the lower carrier's mobility. Such reduction is only observed for larger electric fields (V_{GS} ≃ 0.8 V).

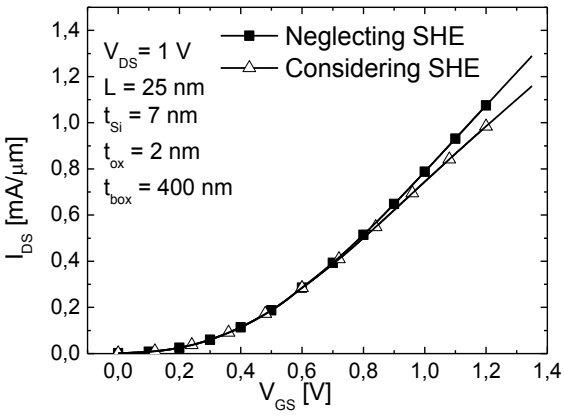

Fig.1. *Drain current (I_{DS}) as a function of the gate voltage (V_{GS}) for V_{DS} = 1V demonstrating the degradation due to the self-heating effect.*

3. Applied Methodology and Results

To extract the thermal resistivity, the hot chuck method has been used [5]. According to this method, simulations neglecting SHE are performed for different temperatures (300, 350, 400, 450 and 500 K) and the data is superimposed with the one of the simulated curve considering self-heating effect. One can determine the approximate channel temperature as the temperature at the intersection points for each V_{DS}. The I_{DS} vs. V_{DS} curves neglecting SHE for different temperatures and considering the self-heating at 300 K for the 25 nm-long transistor with t_{box} =10 nm are presented in Fig. 2 for $V_{GS} = V_{TH} + 0.8$ V, where V_{TH} is the threshold voltage that ranges from 0.53 to 0.49 from the thinnest to the thickest t_{box}. By plotting each point at function of the normalized power, the slope indicates the value of the thermal resistance as illustrated in Fig. 3 (top). The thermal resistance has been extracted for devices of different t_{box} and its dependence on the buried oxide thickness is presented in Fig. 3 (bottom). As it can be noted in the figure, R_{TH} seems to vary nearly linearly with the buried oxide thickness, although its dependence on t_{box} seems to be steeper for thinner buried oxide layers.

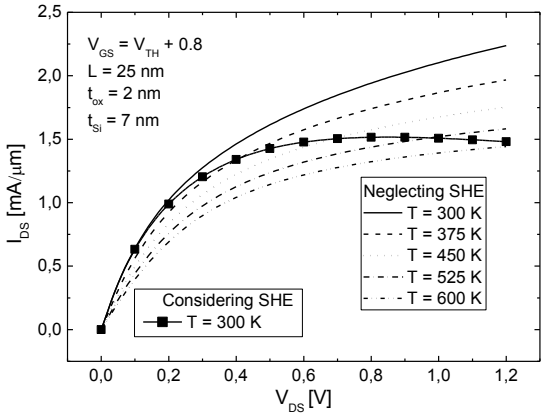

Fig.2. *Drain current as a function of the drain voltage considering and neglecting SHE for the application of the Hot Chuck method.*

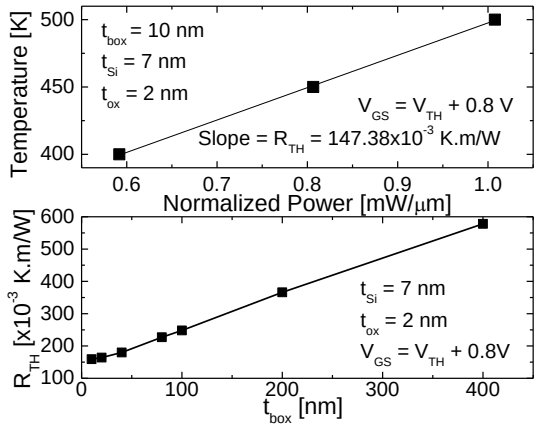

Fig.3. *Device temperature as a function of the normalized power for a 400 nm-t_{box} transistor (top) and thermal resistance as a function of t_{box} for different devices.*

In Fig. 4, it is shown the ratio between I_{DS} considering and neglecting the self-heating as a function of V_{DS} for devices with different t_{box}. As one can observe, for transistors with thicker buried oxide, the ratio between both I_{DS} is smaller than the unit for the whole V_{DS} range, indicating that the mobility reduction due to SHE is responsible for the I_{DS} degradation. On the other hand, for thinner t_{box}, I_{DS} presents an increment, indicating that the impact ionization becomes more influent than the self-heating effect.

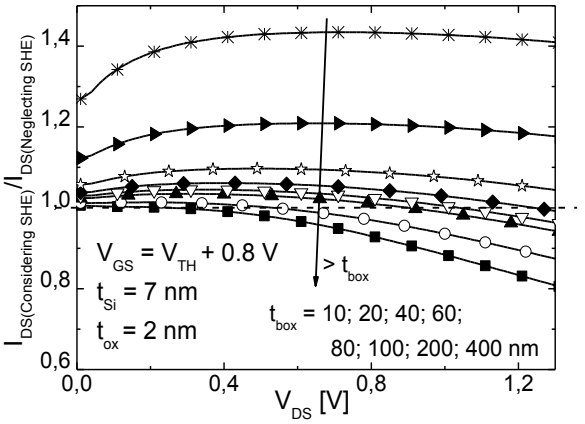

Fig.4. *Ratio between the drain current considering and neglecting the SHE ($I_{DS(ConsideringSHE)}$/ $I_{DS(NeglectingSHE)}$) as a function V_{DS} for devices with different buried oxide layers.*

4. Conclusions

This work has evaluated the impact of the self-heating effect shown by UTB SOI transistors with the reduction of the buried oxide layer thickness. The overall analysis has been performed through the application of the hot chuck method and it has been observed that the thermal resistance presents a nearly linear dependence on the buried oxide thickness, which seems to slightly increase for devices with thinner t_{box}. Finally, it could be seen that while the self-heating effect provokes a drain current reduction for thicker t_{box}, for thinner ones it is overcome by the impact ionization, which leads to the increase of I_{DS}.

Acknowledgments

The authors thank the Brazilian funding agencies CAPES, CNPq and FAPESP for the financial support and the Centro Universitário FEI for the sponsorship.

References

[1] K.K. Young, *IEEE TED*, v. 36, n. 2, pp. 399–402, 2002.
[2] J.P. Colinge, Silicon-on-Insulator Technology: Materials to VLSI, Kluwer Academic Publishers, 3rd ed., 2004.
[3] J.P. Colinge, FinFETs and other multi-gate transistors, Springer, 2007.
[4] S. Makovejev *et al.*, in Proc. *Ultimate Integration on Silicon, ULIS*, 2012
[5] C. Fiegna, *et al. IEEE TED*, v. 55, n. 1, pp. 233–244,2008.
[6] N. Rodriguez, *et al.*, in Proc. *IEEE SOI conference*, 2011.
[7] Sentaurus Dev. User Guide, Synopsys, 2013.