Minimal Design of a Reconfigurable Carbon Nanotube FET

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1. Abstract

Multifunctional transistors present a promising strategy to further scale electronic devices. They can be reconfigured by an electrical signal to provide n or p-type characteristics. This paper gives performance projections of a minimal single gate (1G) carbon nanotube (CNT) reconfigurable (R) field-effect transistor (FET). The only gate controls the charge injection into the conduction or valence band through a Schottky barrier. Simulated figures-of-merit include the sub-threshold slope, the on/off current ratio and the peak transconductance.

2. Introduction

Nanoelectronics explores the idea of self-assembled structures for the fabrication of electronic devices. CNTs are especially interesting since their cylindrical geometry allows optimal electrostatical control of the channel potential. Moreover, CNTs provide high carrier velocity for high current drive, transconductance and cut-off frequency [1]. Since chemical doping in aggressively scaled devices will be difficult to control, carbon based electronics relies usually on Schottky-barrier (SB) FETs with intrinsic channels. Interestingly, SB-FETs allow electrostatical doping of the channel, paving the way to reconfigurable FETs, which deliver n- and p-type behavior depending on a volatile electrical programming signal. Electrostatical doping is achieved by modulating the tunneling transmission through the SB between the source metal and the nanotube channel. In order to allow symmetric n/p characteristics, the work function of the source and drain contacts should be aligned to the mid-energy of the CNT band gap (E_{gap}). First circuit designs based on n/p reconfigurability on transistor level (fine grain) have been already studied [2-4].

We present here performance projections for a minimal 1G-CNTRFET. The channel length is large to facilitate experimental verification. We solve the drift-diffusion equations coupled to the three dimensional Poisson equation. The numerical solver is implemented in the in-house simulation framework COOS [5].

3. 1G-CNTRFET

The schematic of the investigated transistor is depicted in Fig. 1. Catalytic growth of CNTs leads typically to diameters of 1 to 3nm. A value of 2.4nm gives E_{gap}=0.36eV, which is advantageous for high on currents. The effective charge carrier mass is small and

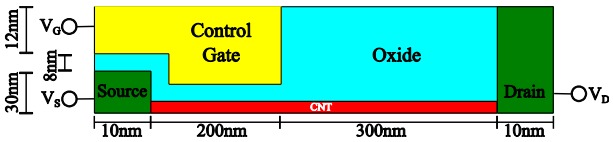

Fig.1: *Architecture of the 1G-CNTRFET.*

amounts to $0.0328m_0$ for both electrons and holes. An 8nm layer of HfO_2 serves as insulating gate capacitor oxide. The control gate overlaps with the source contact to give optimal control of the desired charge injection through the SB. The drain contact is elongated since the fringe fields help to promote n- or p-type behavior exploiting the fact that V_{GS} and V_{DS} share the same polarity. A similar reduced design omitting any program gates has been recently reported [6].

The working principle of the 1G-CNTRFET is best explained with the band diagrams shown in Fig. 2. The transistor is reconfigured from n to p by changing V_{GS} from positive to negative (a↔c). Depending on polarity the source injects electrons into the conduction or holes into the valence band. The transistor is switched off by choosing $V_{GS}/V_{DS}\leq 0$ (a↔b). As a result, the increased SB width effectively prohibits tunneling and the channel turns intrinsic. The influence of the fringe fields on the channel potential is clearly visible.

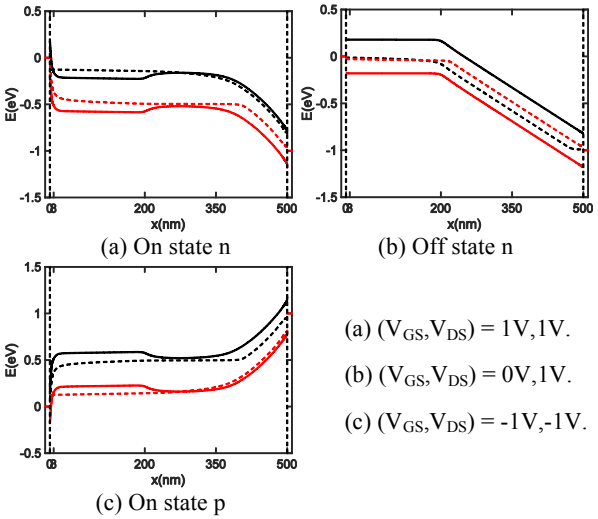

Fig.2: *Band diagrams for three different bias points. Dashed lines indicate the quasi Fermi level for electrons and holes.*

4. Results

Projected electrical characteristics of the 1G-CNTRFET are summarized in Figs. 3-5. Indeed, the transistor can be successfully reconfigured as p- or n-

type FET. The transistor gives symmetric n/p transfer and output curves due to (i) the alignment of the work function of the source and drain metal to the mid-energy of the CNT band gap and (ii) the similar effective mass of electrons and holes. Only n/p symmetric RFETs are useful for circuit design. The large CNT diameter leads to a small band gap and therefore small SB heights. Consequently, the current carrying capability of a single CNT is high amounting to 10.2µA/CNT at a bias point (V_{GS},V_{DS}) = (2V,2V). Therefore, a large current per gate width of 102µA/µm is expected for a CNT technology with a moderate tube density of 10 CNTs/µm, sufficient to drive high performance applications. On the other hand, the small band gap leads to a large leakage current since intrinsic charge carrier densities are relatively high. The projected I_{off} equals 0.1µA/µm, resulting in a too high standby power. Moreover, the sub-threshold slope SS does not reach the 60mV/decade limit stressing the difficulty to switch off the transistor.

Fig. 5 shows the bias dependence of the trans-conductance gm for the n-type configuration. The peak value of gm is high and will also scale with CNT density. Interestingly, gm exhibits an unusual type-independent bias dependence with two peaks, which is the result of two geometry-related competing effects: With gate bias, (i) the width of the SB decreases and (ii) a potential step develops at the end of the gate, see Fig. 2(a) and (b). Such a different shape of the transfer characteristic may be explored in new circuit topologies. The output characteristics exhibit also an unusual S shape leading to a high channel resistance at low bias. Finally, Table I summarizes key parameters at V_{DS}=1V.

Table I. *Figures-of-merit of the n- and p-type 1G-CNTRFET.*

SS	I_{On}(1V)/I_{Off}(0V)	Peak gm
158 mV/dec	369	11 µS

5. Conclusions

We have investigated a minimal design of a CNTRFET. Main features of the transistor architecture are a single source-sided gate and an elongated drain contact to apply large fringe fields to additionally control the channel. The common polarity of the drain and gate bias selects the n/p configuration of the transistor. The transistor exhibits symmetric n/p characteristics. The designed transistor delivers sufficient current drive but a too high standby power. Further optimization is beyond the scope of the present work but a comparison to various (non) reconfigurable transistor geometries employing differently sized CNTs is currently prepared. The simple design considered here should facilitate experimental verification of the theoretical projections allowing calibration. Simulated RFET characteristics serve as basis for compact model development enabling circuit simulations and the exploration of multi-functionality of CNTRFETs for unconventional data processing.

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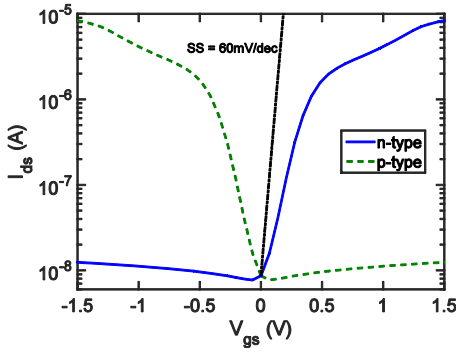

Fig.3: *Transfer characteristics for V_{DS} = 1V*

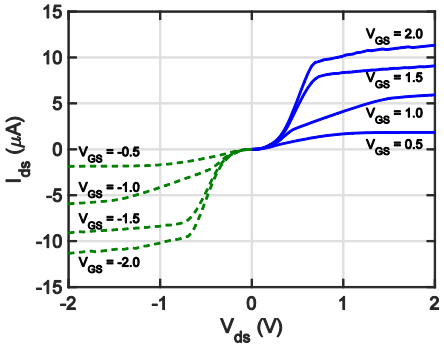

Fig.4. *Output characteristics for different V_{GS}.*

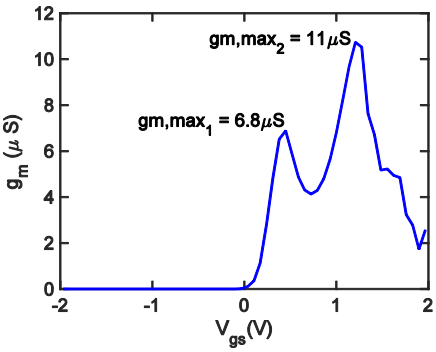

Fig.5. *Bias dependent transconductance for the n-type mode*

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