A Bluetooth Low Energy system analysis for low power applications

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1. Abstract

This work presents the system analysis development of a 2.4GHz ISM receiver for bluetooth version 5.0 standard with low energy mode operation for low power applications. The system is composed by a Radio-Frequency (RF) Front-end with a Low Noise Amplifier (LNA) and two I/Q mixers, baseband filtering stage, Variable Gain Amplifier (VGA) and Analog to Digital Converter (ADC). The system design is based on a 0.5V supply and 10mW overall power consumption constraint. The base calculations for the circuit blocks design are presented, as a viability proof for the project.

2. Introduction

The recently increasing Internet of Things (IoT) applications rely on highly integrated, compact and low power consumption devices, that usually have battery supplies or energy harvesting, demanding also low supply voltage capabilities [1]. Low voltage operation characteristics impose a new approach on the circuits topology choice, where stacked and high voltage needing devices are avoided. Low power operation also include reduction on current values, and current paths.

Low power IoT applications usually are based on short and medium range communication standards, with low data rate, a category in which wireless personal area networks (WPAN) and wireless local area networks (WLAN) are included, one of the most used standards is the bluetooth, with a low energy operation mode available [2].

3. Receiver System

Figure 1 shows the overall receiver system with its circuit blocks, it uses a heterodyne architecture with low-IF characteristic, for the narrow-band bluetooth radio protocol. Bluetooth operates in the 2402 - 2483.5 MHz frequency range, with 40 channels with 1 MHz bandwidth or 2 MHz (depending on system architecture) spacing each other, with GFSK modulation with 0.5 index, and -70dBm sensitivity constraint. Those specifications allow the calculation of the noise and linearity performance constraints for the system.

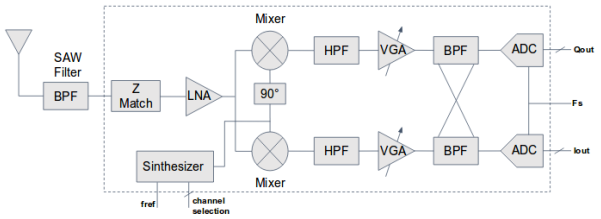

Fig.1. *Receiver system block diagram*

From the demodulation algorithm considered, the Signal-to-Noise Ratio (SNR) can be determined, based on standard requirements, the SNR is calculated for the Bit Error Rate (BER) presented in equation 1. We also set a Intermediary Frequency (IF) of 2 MHz for the baseband part of the system. The internal noise of the receiver is then calculated, based on the bandwidth considered, as shown in equation 2.

$$BER \leq 10^{-3} \tag{1}$$

$$N_s = 10log(kTB) = -114dBm \tag{2}$$

BLE standard requires a minimum sensitivity on the input, a value of -80dBm is considered. With the values obtained before, and considering an insertion loss (IL) of -2dB, the maximum noise figure of the system can be calculated, as shown in equations 4 and 5.

$$NF = S_{in} + IL - N_s - SNR_{out,min} \tag{4}$$

$$NF = -80dBm - 2dB - (-114dBm) - 12dB = 20dB \tag{5}$$

The noise floor (n_{floor}) can be estimated by equation 6, and makes IIP_3 calculation, as shown in equations 7 and 8, where P_{int} represents the in-band blockers power.

$$n_{floor} = N_s + NF = -94dBm \tag{6}$$

$$IIP_3 = \frac{1}{2}(3P_{int} - n_{floor} - \Delta) \tag{7}$$

4. Low Noise Amplifier

This block performs a key role in the receiver chain. As the first block in the signal path, it is responsible to applies moderate gain while adding the smallest amount of noise. For a BLE receiver the LNA topology must

respect the main specifications as lower noise figure, moderate gain, linearity and also works with a 0.5V supply, which is the biggest challenge for the LNA design.

For this system, the SAW filter loss and receiver parameters such as IIP3, 1dB Compression Point, minimum sensitivity and noise figure have to be considered for the LNA design. Topologies including minimum number of stacked devices are preferred because of the low supply voltage, and minimum number of current paths, because of low power requirements.

Equation 8 shows the Friis relation, imposing that the noise from a circuit block is attenuated by the product of preceding gain values, hence the LNA is the block that demands most attention with noise response.

$$N = N_1 + \frac{N_2 - 1}{A_{12}} + \frac{N_3 - 1}{A_{12} \times A_{22}} \quad (8)$$

Most LNA topologies consists in a main amplification transistor, usually in common source configuration, that may or not be followed by a cascode stage. Equation 9 shows the relation to determine the optimum value for this transistor width [5].

$$W_{opt} \approx \frac{1.5}{\omega_o L C_{ox} R_s Q_{in,opt}} \quad (9)$$

5. I/Q Mixer

The first proposed approach for the mixer is to improve the classical double balanced gilbert cell to reduce the number of stacked devices, by using inverters [6].

Some works in low voltage design also use passive mixers, as a simple implementation, reducing supply requirements, power consumption and die area, with the trade-off of gain reduction and noise increasing [7].

6. High Pass Filter

Responsible for the first IF signal filtering, with the main objective of reject the image part of the signal.

7. Variable Gain Amplifier

This amplifier adjusts the signal level to satisfy the requirements of the ADC full scale level, avoiding signal saturation and delivering maximum dynamic range.

8. Complex Filter

A second stage filtering, using complex technique that behaves as a band pass filter, using only low pass filter blocks working at low frequency. This filter makes the coupling of the VGA signal with the ADC. Also, this filter attenuates others frequencies components near to the desired signal, enhancing the SNR at the ADC input.

9. Analog to Digital Converter

Converts the analog IF signal to discrete digital signal in the form expected by the demodulator. Phase ADC's have been used for low power applications due its direct quantization of IF signal, turning unnecessary to use 2 ADC's, also the BER performance is increased [8].

7. Conclusions

This work has the objective of analyze and guide the implementation of a Bluetooth Low Energy system, using the version 5.0 core specifications. By the analysis results obtained, the blocks design can be developed, validating the calculated performances to fabricate the system as a SoC.

Acknowledgments

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