Process simulation of UTBOX SOI Devices for 1T-DRAM Memory Application

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1. Abstract

In this paper, Ultra Thin Box Silicon On Insulator devices (UTBOX SOI) will be studied through numerical and process simulations. These devices can also be used as a memory cell 1T-DRAM (single transistor dynamic random access memory). The drain current (ID) and transconductance (gM) will be analyzed for different gate voltage (VG) and Drain Voltage (VD) on linear and saturation region. The results indicate that simulated devices showed variations in the drain current for different voltage values.

2. Introduction

SOI technology has emerged as an alternative improvement of CMOS (Complementary Metal Oxide Semiconductor) [1], and its manufacture is used a thin layer of silicon oxide which is isolated from the device substrate. This proposal isolation between device and substrate provided by the insulating layer is responsible for the attenuation of parasitic effects in MOS technology.

UTBOX SOI devices are very promising for further downscaling of one transistor and no capacitor 1T DRAM [2, 6]. The presence of the memory effect (floating body), which relies on holes injection into the device substrate can be assessed by the device latchup/hysteresis measurements.

The conventional latchup definition states that this phenomenon is an extreme case of the floating body effects and occurring at a sufficiently large drain to source bias [1]. The latchup effect is usually reported in partially depleted (PD) SOI, although it is also shown in FD SOI with or without UTBOX [4, 5].

With different bias voltage and current applications at the transistor terminals, differential equations are generated within the software environment.

To solve the equations, the mathematical models of Gummel and Newton, along with the Poisson equations, were chosen, through a decoupled procedure. The reason for this is due to the less effort of processing of the computer prepared to the simulation, using these mathematical methods.

With the validation of the results, we compared those obtained within the simulation with those achieved experimentally in IMEC (Interuniversity Microelectronic Center) – Belgium.

The simulation can be proven at the moment when the manufacturing process was allied with the introduction of electricity in the component and the desired curves were obtained.

3. Methodology and Results

In this work, the experimental data were obtained through simulations within the Athena [5] software. Within this was generated code required for the transistor to respond to different voltages applied to the drain (VD).

The n-channel device analyzed, in Figure 1, have been fabricated on SOI substrates with a 20 nm buried oxide (TBOX) and Si film (TSi) 20 nm. The channel is undoped, L = 170 nm and the gate dielectric (TOX) consists of 2.5 nm SiON. More process details can be found in ref [6, 7].

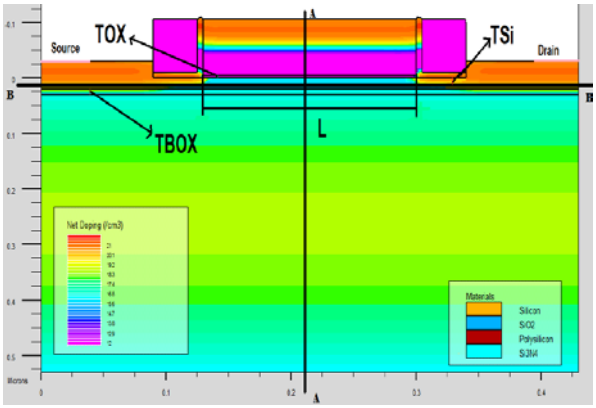

Fig.1. *SOI UTBOX nMOSFET net doping indicating Source, Drain, line A–A, line B–B and different parameters like TOX, TSi and the channel length (L).*

According to the data [6], obtained in the laboratory of the IMEC, Belgium, it was possible to define the doping scales necessary for the formation of the studied component. According to the Fig. 1, source and drain are more doped than the substrate, as well as the source. In addition, in order to obtain a functional check of the device, it was necessary, through the ATLAS software, to plot the current curve in the drain as a function of the gate voltage (ID x VG).

About the doping curves, the software Atlas did the cuts according to the coordinates of figure 1. This is shown in Fig. 2.

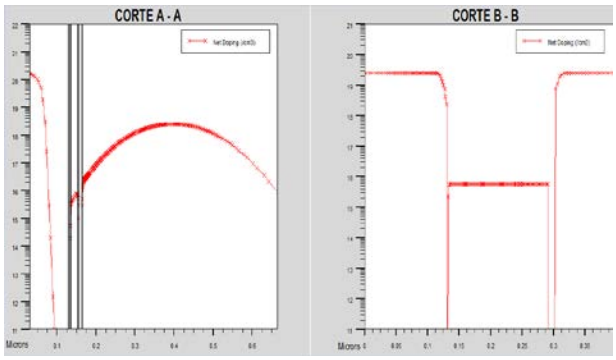

Fig.2. *Doping Concentration as a function of length (line A–A, line B–B indicating in Fig.1).*

So, the code required for the transistor to respond to different voltages applied to the drain (VD) was generated. The code defines drain currents (ID) as a function of gate voltage (VG). VD is variable and VG varies from -2 V to 2 V, every 0.2 V. Figures 3 and 4 show the curves of drain current (ID) versus gate voltage and transconductance (gM) versus gate voltage for simulated device. As expected, when VD is higher, drain current and transconductance is also higher.

4. Conclusions

Simulated device showed variations in the drain current for different voltage values. When the drain voltage increase the drain current is higher, as expected.

An in-depth study of SILVACO software was crucial for the calibration/validation of simulations from experimental results of state-of-the-art and conventional transistors.

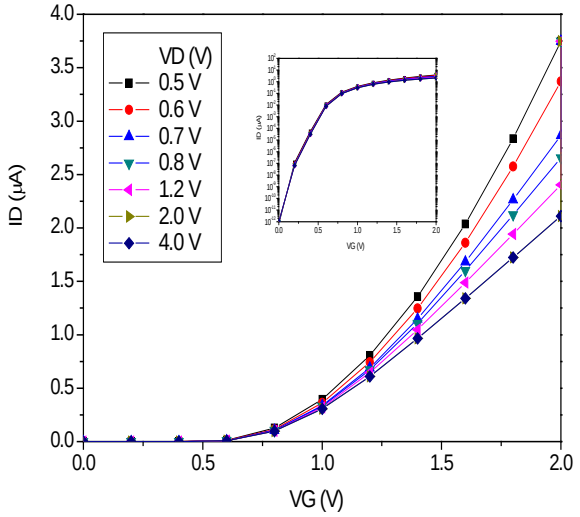

Fig.3. *Drain current (ID) as a function of gate voltage (VG) for SOI UTBOX nMOSFET.*

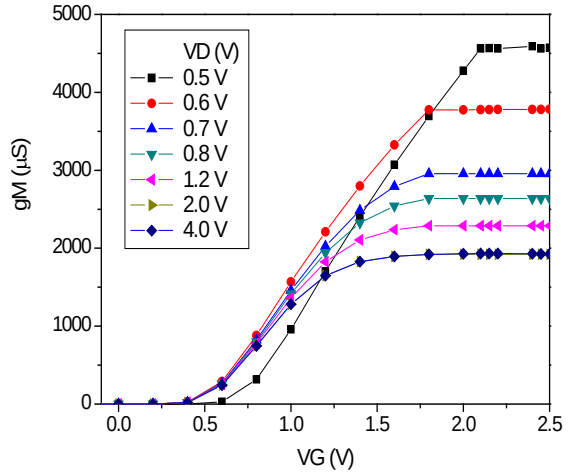

Fig.4. *Transconductance (gM) as a function of gate voltage (VG) for SOI UTBOX nMOSFET.*

Acknowledgments

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