Modelling of MOS devices for solar energy harvesting

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1. Abstract

Solar energy harvesting is the capture of some quantities of light indoor or outdoor to convert in electricity [1]. It uses the photovoltaic effect of the silicon and power availability changes according to the positioning of the solar cell with respect of the energy source. For instance, outdoor energy harvesting is easily doable thanks to the big power generated by solar irradiation even under overcast conditions, while indoors there are more constraints due to the lower light intensity available. A simple solar energy harvesting method is to use the carriers photogenerated from MOS solar cells, which are excellent devices..The generated carriers can flow through a thin (2 nm) silicon oxide by means trap-assisted tunneling. In this work, it is presented the modelling of the trap-assisted tunnelling with the aid of the IxV characteristics.

2. Modelling

The tunneling current density in the oxide can be written by the Equation 1 [2, 3]:

$$J = J_D + J_I + J_T \tag{1}$$

where J_D is the direct tunneling, J_I is the inelastic tunneling of electrons through traps inside the gate oxide and J_T is the tunneling of electrons into the anode interface states. The J_D component is less significant in thicker oxides with high concentration of traps.

J_I component is given by equation 2, to negative gate voltages [2]:

$$J_I = q\sigma_I N_{tr} v_{th} T p_s \tag{2}$$

where q is the electron charge, σ_I is the trap capture cross section in inelastic tunneling current, N_{tr} is the trap density, v_{th} is the thermal velocity, T is the tunnel probability from a trap to the substrate and p_s is the interface substrate hole concentration. T is the tunnelling probability and depends on the trap position (x_{trap}), according to the Equation 3 as follows:

$$T = \exp\{-\frac{4\pi}{h}\int_{x_{trap}}^{0}[2m^*(\Phi_{bar}(x)-\Phi)]^{\frac{1}{2}}dx\}$$

Or, discretizing the integral, one obtains:

$$T(\Phi) = \exp\{-\frac{4\pi}{h}\sum_{i=1}^{n}[\sqrt{2m^*(\Phi_{bar}-\Phi)}]\Delta t\},$$

$$\Delta t = \frac{x_{trap}}{n} \tag{3}$$

where

$$\Phi_{bar}(x) - \Phi = q\phi_f + 0{,}55 + \chi_{Si} - qV_g - q\frac{x_{trap}}{t_{ox}}V_{ox}\left(\frac{x}{t_{ox}}\right) - \Phi_{ox},$$

Φ is the energy level, Φ_{bar} is the energy level in the oxide, as a potential barrier, ϕ_f is the Fermi potential, V_{ox} is the electric potential difference in the oxide, V_g is the gate voltage, χ_{Si} is the electronic affinity of the silicon and t_{ox} is the oxide thickness.

On the other hand, J_T (current into anode interface states) component is given by Equation 4 [2]:

$$J_T = C\int_{\Phi_{Cg}}^{\Phi_{Cs}} \ln(1+\exp(\frac{\Phi-\Phi_f}{k_B T}))P_T(\Phi)\sigma_T D_{it}(\Phi)d\Phi$$

$$C = \frac{q n_m m^* k_B T}{2\pi^2\hbar^3} \tag{4}$$

for:

- n_m band degeneracy;
- m^* effective mass;
- k_B Boltzmann constant;
- T temperature in Kelvin;
- Φ_{Cs} conduction band edge of the substrate;
- Φ_{Cg} conduction band edge of the gate;
- $\hbar$ reduced Planck constant;
- P_T tunnel probability in TEDit current;
- σ_T trap capture cross section to TEDit current (σ_T not equal to σ_I);
- D_{it} interface state distribution.

For positive gate voltages, electrons are the predominant carriers at the interface substrate (n_s) and J_I can be described by Equation 5 as follows:

$$J_I = q\sigma'_I N_{tr} v_{th} T n_s \tag{5}$$

where the trap capture cross-section σ'_I is not equal to σ_I of the previous case.

3. Results

Table 1 shows the effective trap positions from the

metal gate as the reference in the 2nm-thick silicon oxides and their concentrations, respectively. Samples are 300x300 µm in area and they were submitted to different thermal oxidations (700°C and 850°C) in ultrapure oxygen. Al was defined as the metal gate.

Table 1. *Trap concentrations and average positionsin the samples adjusted according equation 2.*

Sample	**Trap concentration (cm^{-3})**	**Trap position (Å)**
(A)	10^{17}	13.2
(B)	10^{15}	8.0

Sample A was treated at700°C while sample B was treated at 850°C. It is worth of note that the higher the temperature of treatment, the lower the trap concentration. This is understood considering that higher temperatures favors the completion of the chemical bonds in the oxide.

Figures 1 to 3 show a comparison between measured (experimental) and calculated (modeled) I-V Characteristics. The trap capture cross section was the adjusted parameter for the modeling.

Figure 1 below uses $\sigma_I = 5.78 \times 10^{-8}$ cm^{-3} and x_{trap} = 13.2 nm as adjusting values.

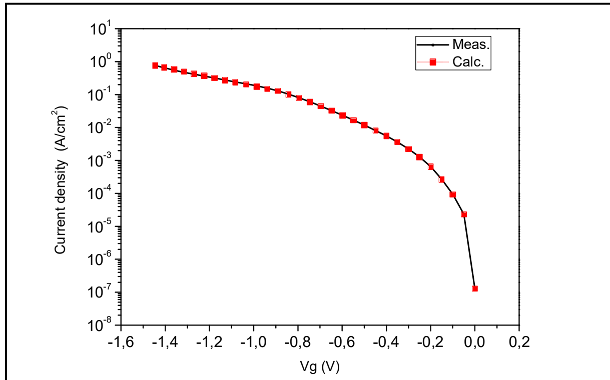

Fig.1.*Fitted I-V Characteristic in the accumulation mode(V_g< 0) for the gate oxide grown at 700°C*

Figure 2 uses $\sigma_I = 3.82 \times 10^{-10}$ cm^{-3} and x_{trap} = 8.0 nm as adjusting values

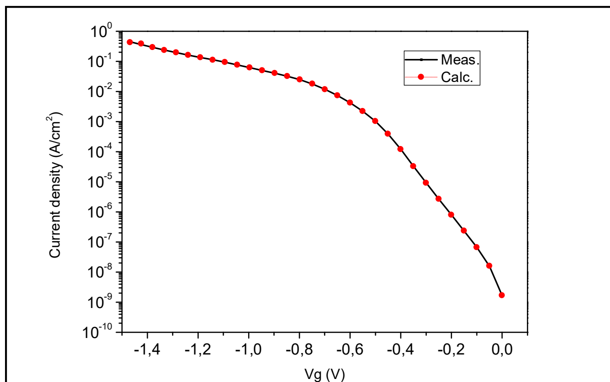

Fig.2.*Fitted I-V Characteristic in the accumulation mode (V_g< 0)for the gate oxide grown at 850°C.*

On the other hand, Figure 3 shows measured and calculated curves IxV in inversion mode ($V_g > 0$), using $\sigma'_I = 9.16 \times 10^{-19}$ cm^2 and x_{trap} = 3.0 nm.

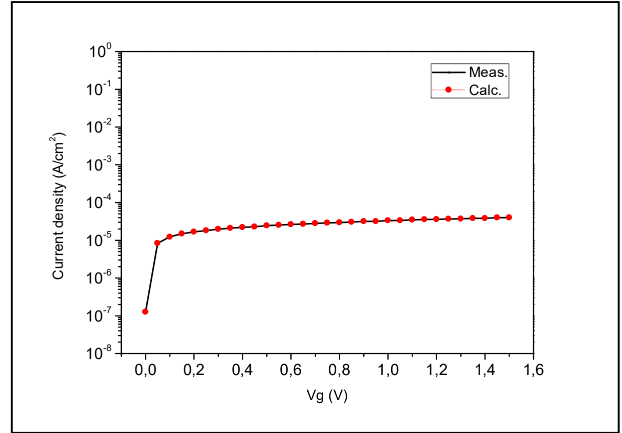

Fig.3.*Fitted I-V Characteristics in the inversion mode (V_g> 0) for the gate oxide grown at 700°C*

Results of the figures 1 and 2 show excellent fits of the equation 2 to the I-V Characteristics in the accumulation mode. Also, Figure 3 also shows an excellent fit of the equation 4 to the I-V characteristics in the inversion mode.

4. Conclusions

. In this work, it was presented the fitting of the trap-assisted tunnelling model [2,3] to the IxV characteristics of MOS cells with gate oxide 2-nm thick.

The results showed excellent fits using the trap-assisted tunnelling model to the I-V Characteristics in the accumulation and inversion modes.

Acknowledgments

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References

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