

BE SOI MOSFET: A very simple reconfigurable SOI transistor

L. S. Yojo, R. C. Rangel, K. R. A. Sasaki and J. A. Martino
 LSI/PSI/USP – University of Sao Paulo, Sao Paulo, Brazil
 e-mail: l_yojo@hotmail.com

1. Abstract

This paper presents the new BE (Back Enhanced) SOI MOSFET, a planar device fabricated at Integrated System Laboratory (LSI) from University of São Paulo (USP), Brazil, which has the property of operating both as a n-type or as a p-type transistor. Also, the working principle is explored by investigating experimental and simulated data.

2. Introduction

A reconfigurable transistor that can act both as a n-type and as a p-type MOSFET presents a flexibility of operation that may enable better circuit design [1]. Many options use sophisticated fabrication processes and architectures such as nanowires [2,3,4] to obtain a reconfigurable transistor. There are papers that report simulation results [5,6] for this kind of device. In this work we introduce the new BE SOI MOSFET, a device with very simple fabrication processes, no doping step is needed, just conventional photolithography and metal depositions are used [7,8] and has the reconfigurable property.

The BE SOI MOSFET was fabricated at Integrated System Laboratory (LSI) from University of São Paulo (USP), Brazil. It was processed on a 200nm thickness buried oxide SOI wafer with only three conventional photolithography steps and no doping process (the natural doping concentration is 10^{15}cm^{-3}). The final silicon layer and the gate oxide thickness are 10nm each. The source and drain Schottky contacts were made with nickel and the metal gate with aluminum.

Fig. 1 shows the schematic profile of this planar device and the picture of the fabricated device can be seen in fig. 2.

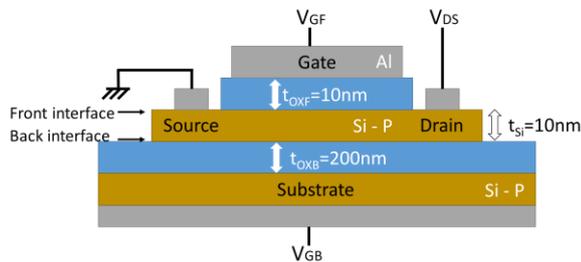


Fig.1. BE SOI MOSFET schematic profile.

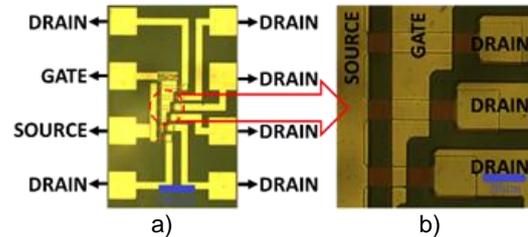


Fig.2. Pictures of the fabricated BE SOI MOSFET. a)array of transistors b)insets of some transistors fabricated at LSI/USP/Brazil.

3. Operation principle

The BE SOI MOSFET has a unique operation principle that enables it to operate like a n-type or a p-type MOSFET transistor, depending on the back gate voltage V_{GB} .

In the case of a BE SOI nMOSFET, the V_{GB} is positive. Therefore, electrons are accumulated at the back interface allowing the current flow from drain to source. Similarly, in the case of a BE SOI pMOSFET the V_{GB} is negative and holes are accumulated at the back interface.

Fig. 3 shows the drain current as a function of the front gate voltage V_{GF} for different V_{GB} . It is possible to note the flexibility of the device that can work as a n-type or a p-type transistor. The higher the $|V_{GB}|$ value, the higher the current level because more charges are accumulated at the back interface.

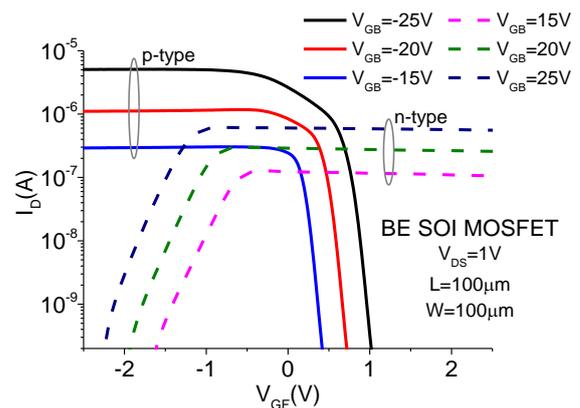


Fig.3. Drain current as a function of the front gate voltage V_{GF} , working like a ptype ($V_{GB} < 0$) and n-type BE SOI ($V_{GB} > 0$).

The current flow is controlled by the front gate electrode. In the case of a BE SOI nMOSFET, if the V_{GF} is enough negative, the silicon layer under the front gate stack is fully depleted and the current is ceased.

Fig. 4 shows the simulation of the band diagram in the off state of the transistor (using Synopsys Sentaurus [9]). The energy barrier seen by the electrons in source/channel region stops the current flow.

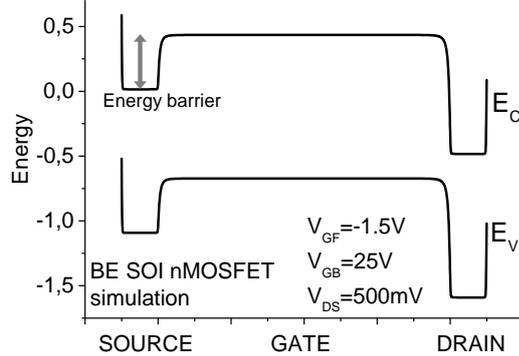


Fig.4. Band diagram simulation (Sentaurus) of the BE SOI nMOSFET.

An analogous behaviour occurs in the case of a BE SOI pMOSFET. If the V_{GF} is enough positive the silicon layer under the front gate stack is fully depleted and the current is ceased. Fig. 5 shows the simulation of the band diagram in the off state of the transistor where the energy barrier seen by the holes in source/channel region stops the current flow.

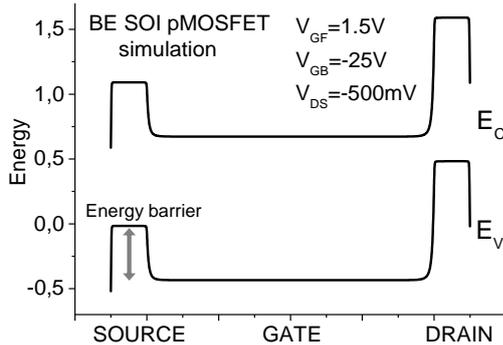


Fig.5. Band diagram simulation (Sentaurus) of the BE SOI pMOSFET.

4. Conclusions

The working principle of the BE SOI MOSFET was explored in this paper. This new device showed a flexible operation principle; depending on the V_{GB} value it is possible to have a n-type or a p-type transistor. The current level presented to be proportional to V_{GB} and the off state of the transistor was explained with simulation results.

This flexible behavior and the simplicity of fabrication make the BE SOI MOSFET an interesting option of device architecture.

Acknowledgments

The authors would like to thanks CNPq and FAPESP for the financial support during the execution of this work.

References

- [1] J. Trommer, A. Heinzig, S. Slesazeck, T. Mikolajick and W. M. Weber, "Elementary Aspects for Circuit Implementation of Reconfigurable Nanowire Transistors," IEEE Electron Device Letters, vol. 35, no. 1, 2014.
- [2] F. Wessely, T. Krauss, U. Schwalke, "Reconfigurable CMOS with undoped silicon nanowire midgap Schottky-barrier FETs," Microelectronics Journal, vol. 44, pp. 1072-1076, 2013.
- [3] A. Heinzig, S. Slesazeck, F. Kreupl, T. Mikolajick and W. M. Weber, "Reconfigurable Silicon Nanowire Transistors," Nano letters, vol. 12, pp 119-124, 2012.
- [4] M. Simon, A. Heinzig, J. Trommer, T. Baldauf, T. Mikolajick, W. M. Weber, "Bringing reconfigurable nanowire FETs to a logic circuits compatible process platform," IEEE Nanotechnology Materials and Devices Conference, 2016.
- [5] T. Krauss, F. Wessely and U. Schwalke, "Electrically reconfigurable dual metal-gate planar field-effect transistor for dopant-free CMOS," 13th International Multi-Conference on Systems, Signals & Devices, 2016.
- [6] C. Navarro, S. Barraud, S. Martinie, J. Lacord, M. A. Jaud and M. Vinet, "Reconfigurable field effect transistor for advanced CMOS: a comparison with FDSOI devices," EUROSOCI-ULIS, 2016.
- [7] R. C. Rangel, J. A. Martino, "Back Enhanced (BE) SOI pMOSFET," Microelectronics Technology and Devices (SBMicro), 2015.
- [8] Martino, J.A. and Rangel, R. C., "BE SOI MOSFET" Patent number BR 10 2015 020974 6, 2015.
- [9] Synopsys TCAD, Sentaurus Device User Guide, Version H-2013.03, Synopsys, Inc, 2013.