Verifying the Interface between a Digital Windowing Block and a Sigma-Delta Analog to Digital Converter

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1. Abstract

This works presents a different way to verify interfaces of AMS and digital components using a Metric Driven Methodology commonly used by the digital verification engineers. The mainly idea is to guarantee the communication between the digital and analog blocks describing the process used to make all the verification. The blocks chosen to the verification process will be Sigma Delta ADC and Windowing. The blocks used in this process was developed by design team of IC-Brazil and are part of Transponder IP block that will compose the Potiguara project along with other blocks.

Keywords— Analog and mixed signal-AMS; Analog Digital Converter-ADC; Windowing;

2. Introduction

The recent CMOS technology evolution presented a higher development of digital circuit designs over analog circuit designs. Also, it happens with verification approaches to digital and analog blocks. Most of this effect has been caused by the CMOS devices channel width reduction, that brings some advantages to digital circuits, such as increase of speed, reduction of power consumption and reduction of area, hence, reduction of cost. When handling signals of analog nature, the use of an Analog to Digital Converter (ADC) is essential to keep most of the processing blocks in the digital domain [6].

In this work, we analyse the interface between data converted by an ADC to a digital window block. We use a Sigma Delta ADC, that takes advantage of Oversampling and Noise Shaping techniques to improve resolution [7]. The Sigma Delta ADC achieves a high resolution with medium signal frequencies.

The section two, will present a brief of mixed signal SoC architecture, focusing in the reception interface and give a highlight in the analog to digital interface. The section three will present verification approach and the verification plan. Following, the section four will present the simulation and the cover experiments achieved/obtained in the interface and the window block. Section five will present the conclusion and future works.

3. SYSTEM DESCRIPTION

The focus of this research is in the reception interface, where digital and analog components exchange data. The interface used is part of a transponder IP, component of Potiguara project developed in order to do the communication among platform data collection and central data collection [1].

Digital, analog and radio frequency (RF) blocks compose the Transponder IP. The main function of the Potiguara SoC is concentrated in the transponder IP which is responsible to receive a signal from a Data Collect Platform (DCP), process the signal, which comprises in remove noise and environmental signal distortion effects, and send it back to a central responsible for analyse all the data collected in the field [1,2].

In this job, an Analog Digital Converter and a Window block were used to make simulations and ensure the communication between both analog and digital worlds.

4. VERIFICATION ENVIRONMENT ARCHITECTURE

The motivation of this research is to develop a verification environment able to analyse and validate the communication between the analog and digital components, which present many challenges.

A. Verification Strategy

The verification strategy performed will be bottom-up and will be divided in two steps. The first step comprises in testing the digital block exhaustively standalone and therefore integrated with the analog block. This action aims in simplify the verification project by reducing the efforts to debug the window block once it is completely and carefully verified.

The verification environment used in the first step is composed by a lot of internal units that are monitor, covers, bus functional models, drivers, agents and checkers as can be seen in Fig. 1.

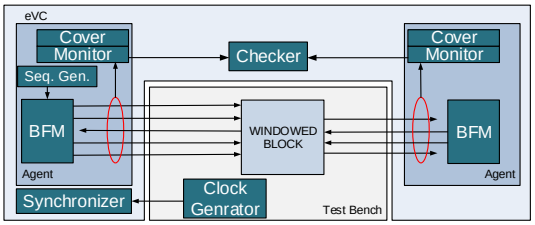

Fig. 1. *Digital Verification Environment for Window Block*

In the second phase, the digital verification environment will be set to work in the passive mode where the stimulus to window block will be generated by the Analog to Digital Converter block. From this step, the stimulus and the simulation will be performed by the analog environment using the Virtuoso and Incisive Simulator Cadence tools. In this kind of simulation, the digital verification environment instantiated is used just to validate the communication between the digital and analog components and validate the data in the communication bus.

B. Verification Environment

The proposed verification environment, used to validate the window block, was developed in object-oriented programming (OOP) combined with e Language to define the verification environment, with orientation to the eRM verification methodology.

In details, the verification environment can be divided in two parts. The first part will be composed by an analog block, designed in a behavioural approach using Verilog-A language that is responsible to generate all stimulus. Moreover, the second part will be a digital verification environment, which is responsible to guarantee the communication protocol between analog and digital block and also make sure that the window block is working as defined in the specification. The used verification environment architecture can be showed in the Fig. 2.

C. Interface Verification

In order to validate the communication between the analog and digital worlds, a lot of expects, which are temporal structures responsible to guarantee communication protocol, were established and inserted in the input monitor located in the interface. Also, the output has expects not covered by the verifications performed, as it will not affect the observed results.

The temporal expression, created to ensure the communication between blocks, should succeed during all the simulation. If a temporal expression fails, the simulation will stop immediately and the simulator will inform a time where the violation happen and show a fault massage.

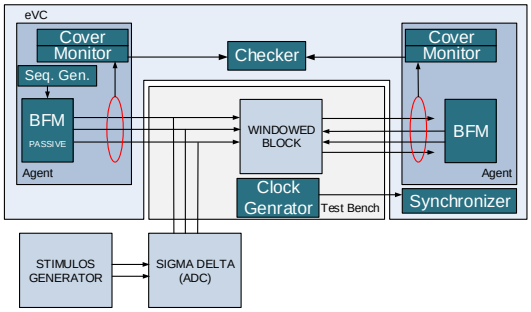

Fig. 2. *Verification Architecture*

D. Functional and Code Coverage

The functional and code coverage are ways used to evaluate how well the design under test was stimulated and define which tests need to be generated in order to reach an acceptable level of verification effort.

An example of a code coverage and functional coverage was taken from the verification process of the design under test is showed in the Fig. 3.

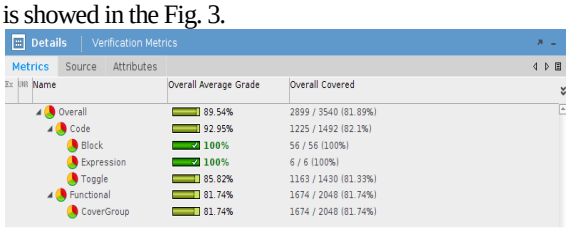

Fig.3. *Code and Functional Coverage*

5. SIMULATION RESULTS

Using the verification architecture proposed in Fig. 2, this research simulates and verifies the analog digital interface through the window verification environment and its temporal expressions.

The simulation mechanism can be depict as: a) Define a verification environment for the window block. b) Test the window block exhaustively and carefully in order to guarantee its perfect functionality. c) Set the window verification environment to work in passive mode. d) Define a generation stimulus, in the analog environment, with eight subcarriers simulating a real scenario. e) Finally, send the generated data to Analog Digital Converter.

The simulation process is quite simple, as can see in the Fig. 4, where is possible to see a waveform with the main inputs and outputs signals. This wave is possible to see the two hanning windows and the signal used to stimulate the analog digital convert component.

With the Incisive Metric Center version 15.10-s007 is possible to observe the code and functional coverages and define which test cases need to generate and which areas need more attention in order to reach a functional and code coverage with a satisfactory level. In the Fig. 3 is possible to observe the coverage results. Exploring the results of coverage, is possible to extract the code coverage that is 92,85% and the functional coverage that is 81,74%. Similarly, the overall coverage taken from the coverage results is 89,54%. The results obtained in the coverage process is quite satisfactory, taking into account the verification time and the code construction styles that has a situations where is not possible to reach during the simulation.

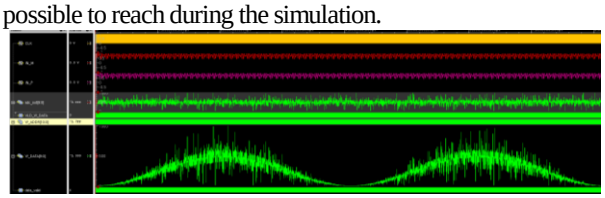

Fig.4. Analog Digital Interface Waveform

6. CONCLUSION AND FUTURE WORKS

This paper presents a way to make a verification of the interface between digital and analog components where in a lot of case represents a challenge in a project of a system on chip. The presented approach has with objective guarantee the communication of the digital and analog blocks is done correctly according with stablished protocol.

The main key benefits to implement this kind of verification includes (i) simulation with digital and analog components, (ii) interface protocol verification based on expects, (iii) real response by analog components, (iv) reusable digital verification environments, (v) function and code coverages.

To sum up, this paper links both the digital and analog components in the same verification environment in order to help the digital verification engineers to validate the interface analog digital ensuring that both are following the protocol. The future research will be focused on faster simulations and improve the reusability of the verification environments.

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