Analysis of different source materials on the drain current of nTFETs

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1. Abstract

In this work, an experimental study of the influence of using different materials on the drain current is presented, using Si, SiGe, Ge and $In_XGa_{1-X}As$ nTFETs. The comparison among the different material showed that the materials with lower bandgap presents higher drain current and also lower onset voltage.

2. Introduction

Tunnel field effect transistors (TFETs) are transistors based on Band to Band Tunneling (BTBT), being capable to reach subthreshold swing (SS) values lower than 60mV/dec [1,2]. However, the Si TFETs suffer from low on-state current (I_{ON}) compared to MOSFETs, and also the device architecture is intrinsically more sensitive to defects causing trap assisted tunneling (TAT), degrading more the SS of TFETs.

In order to increase the BTBT generation, and consequently increase I_{ON} and decrease the influence of the defects, alternative materials with smaller bandgap (Eg) have been studied, such as Ge [3,4] and III-V materials [5-7]. TFETs are not only promising in switching characteristics, but also present good analog characteristics [8-13].

In this paper, an experimental study of the influence of different materials on the drain current is analyzed, comparing Si nTFETs, $Si_{0.73}Ge_{0.27}$ and Ge source heterojunction nTFETs and $In_XGa_{1-X}As$ homojunction nTFETs.

3. Device Characteristics

The analyzed devices are N-type TFETs fabricated in imec/Belgium. These devices can be divided in two different fabrication processes.

The first type are N-type vertical gate all around TFETs with Si Channel and Drain, and with different source materials: Si, $Si_{0.73}Ge_{0.27}$ and Ge. These devices use a top down vertical process flow [14]. The gate stack is composed by a dielectric of 3nm HfO_2 on top of 1nm interfacial SiO_2 and covered by a TiN and amorphous silicon layer. For the Ge source device, a device with 2nm of HfO_2 was measured. The drain region is doped with $2x10^{19}$ As/cm^3, the source is doped with $1x10^{20}$ B/cm^3 and the channel is doped with $1x10^{16}$ As/cm^3. More details regarding these structures can be found in [15].

The second type of devices are n-type $In_XGa_{1-X}As$ homojunction TFETs fabricated using the optimized processing reported by Alian et. al. [7], which follows the original approach from the University of Tokyo [6]. The drain is doped with Si (N++) and the source is doped with Zn (P++) using spin-on glass diffusion. Three different devices were studied, two devices with an uniform $In_{0.53}Ga_{0.47}As$ channel and the other with an 8nm layer of $In_{0.7}Ga_{0.3}As$ on top of the $In_{0.53}Ga_{0.47}As$. The devices with uniform $In_{0.53}Ga_{0.47}As$ channel have different spin-on glass diffusion temperatures, i.e., one at 500ºC (same as $In_{0.7}Ga_{0.3}As$) and the other with higher temperature, 520ºC (HighTempZn), both for 1 minute. The gate stack is composed of 1nm Al_2O_3 and 3nm HfO_2, resulting in an equivalent oxide thickness (EOT) of about 1.5nm, with TiN as the metal gate.

4. Analyses and Discussion

Figure 1 presents the drain current (I_{DS}) as a function of gate voltage (V_{GS}) of the silicon-based nTFET devices, with Si, SiGe and Ge sources. In TFET devices, I_{DS} has mainly three conduction mechanisms, BTBT, present in the I_{ON}, and TAT and Shockley-Read-Hall recombination (SRH), both present in the off-state current (I_{OFF}). When V_{GS} is increased the BTBT component increases due to the higher energy window of overlap between the valence band of the source and the conduction band of the channel. The rise of the overlap also reduces the tunneling length, increasing the BTBT component.

It is noticeable that I_{DS} is increased with a higher Ge amount in the source. This behavior can be explained by the Eg narrowing. For increasing Ge amount in the source, a lower is Eg results, which in turns reduces the tunneling length, increasing the BTBT component in I_{DS}. It is also possible to observe that for the same reason the onset voltage (V_{onset}) is also decreased for higher amounts of Ge.

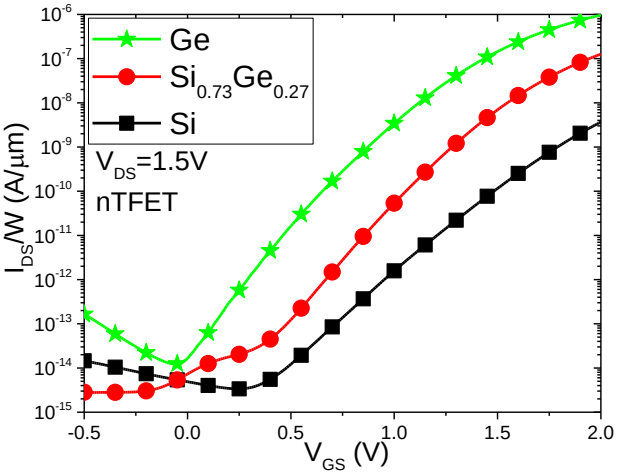

Fig.1. *Normalized drain current as a function of gate voltage of Si, SiGe and Ge source nTFET devices.*

The activation energy (E_a) as a function of V_{GS} for the Si, SiGe and Ge nTFETs is shown in figure 2, which can be determined by the Arrhenius plot [12]. E_a is representative of the conduction mechanism in TFET devices [12,15]. As BTBT is the conduction mechanism less influenced by the temperature in TFETs [12], the lower E_a is, the higher is the BTBT component in a TFET. From figure 2, it is possible to observe that for higher Ge amount in the source of the nTFETs, the lower is E_a, giving rise to a higher BTBT component due to its lower Eg. In Si based TFETs, V_{onset} can be acquired considering the V_{GS} necessary to E_a be lower than 0.1 eV [15]. The V_{onset} shift, which is caused by the lower bandgap, is also noticeable in the E_a curve.

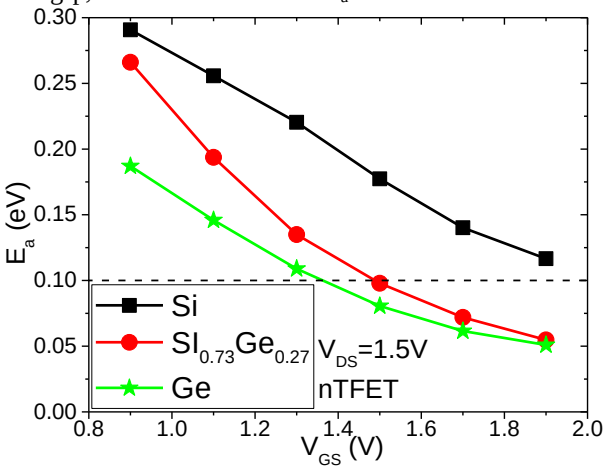

Fig.2. *Activation energy as a function of gate voltage of Si, SiGe and Ge source nTFET devices.*

Using $In_XGa_{1-X}As$ in nTFETs allows to reach even higher current values, as can be observed in figure 3, presented in [16], due to its low Eg, which increases I_{ON} and also decreases the subthreshold swing. These InGaAs nTFETs have been optimized and exhibit subthreshold swing values lower than 60 mV/decade in [17]. Figure 3 presents a comparison between the $In_{0.53}Ga_{0.47}As$, $In_{0.7}Ga_{0.3}As$, and $In_{0.53}Ga_{0.47}As$ channels with higher diffusion temperature (HighZnTemp). It is known that for increasing In amount Eg in an $In_XGa_{1-X}As$ TFET reduces, resulting in a higher I_{ON} for the $In_{0.7}Ga_{0.3}As$ device.

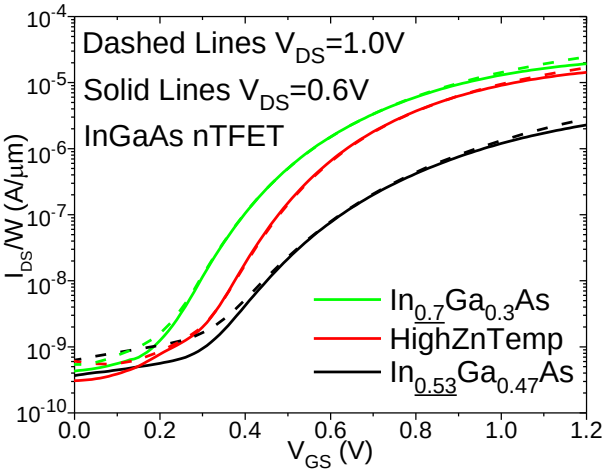

Fig.3. *Normalized drain current as a function of gate voltage of $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$ nTFET devices [16].*

The HighZnTemp device presents a higher BTBT component due to the increase of the active doping concentration, which reduces the tunneling length.

Figure 4 presents the Ea for the InGaAs studied devices [16]. From this figure, one can notice that the Ea values for the $In_{0.7}Ga_{0.3}As$ and the HighTempZn are lower than for the $In_{0.53}Ga_{0.47}As$ channel, showing that these devices presents a higher BTBT component.

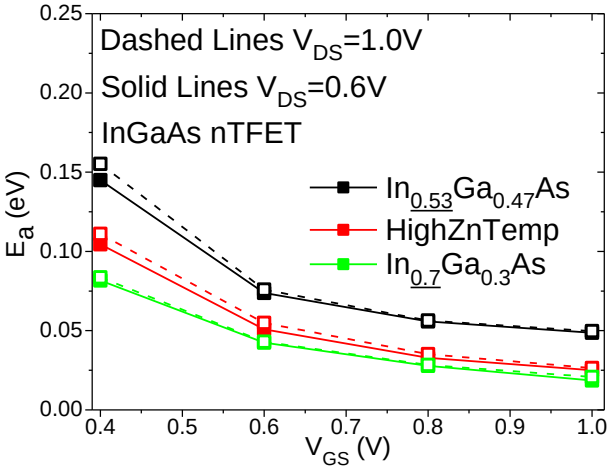

Fig.4. *Activation energy as a function of gate voltage of $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$ nTFET devices[16].*

5. Conclusions

This work presents an experimental study of the influence of using different materials on the drain current, using Si, SiGe,Ge and $In_XGa_{1-X}As$ nTFETs. Using a higher amount of Ge, the bandgap is reduced, decreasing the tunneling length and improving BTBT. A similar effect of improving BTBT occurs for InGaAs devices, improving even more for a higher In concentration. For both increased concentration of Ge and In a decrease of the onset voltage is also noticeable. Silicon TFETs do not show optimized subthreshold characteristics, however, using $In_{0.7}Ga_{0.3}As$, a sub 60mV/dec SS has been obtained.

Acknowledgments

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