Silicon Thickness and Ground Plane Influence on Threshold Voltage and Subthreshold Swing of UTBOX and UTBB SOI nMOSFETs

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1. Abstract

This paper presents the influence of the silicon thickness (t_{si}) on the threshold voltage (V_T), subthreshold swing (SS) and drain induced barrier lowering (DIBL) of ultra thin buried oxide (UTBOX) and ultra thin body and buried oxide (UTBB) SOI nMOSFETs devices. This analysis presented a reduction of the values of these parameters for decreasing t_{si}. The Ground Plane (GP) influence on these parameters was also analysed, but it was noted that the GP did not affect the DIBL, only the V_T and SS values, presenting a higher value when comparing with the device without GP and with the lowest t_{si}.

2. Introduction

In order to follow Moore's law and to improve the performance of the devices it is necessary to reduce their dimension, either in planar technology (UTBB) or tridimensional (FinFET). While the dimensions are being reduced, some effects become more pronounced, such as the short channel effect (SCE) on devices with short channel length [1].

To investigate these effects and to understand their impact on the performance, UTBOX and UTBB SOI nMOSFETs devices were studied. These technologies present high speed, low power and better control of SCE.

Fig. 1 presents a schematic of the two SOI technologies; for a silicon thickness (t_{si}) $\leq$ 50 nm it can represent an UTBOX device, and when t_{si} and the buried oxide (t_{oxb}) have both thicknesses $\leq$ 20 nm, it represents an UTBB device. For the latter a ground plane (GP) implantation can be used to reduce the depletion region that is formed under the buried oxide, resulting in a larger effective thickness [2-4].

This paper presents an analysis of the influence of t_{si} on subthreshold parameters. Three different devices were studied, with two different t_{si} values and with and without GP and with a channel length from 1µm down to 120 nm.

3. Experimental details

The studied UTBOX SOI nMOSFETs have t_{oxb}=10 nm, t_{si}=50 nm, gate oxide (SiO_2) thickness of 5 nm, the gate material is TiN, the channel width (W) is 1µm and four channel lengths: 1µm, 250, 150 and 120 nm. This device has no GP implantation, and throughout this paper it will be called split A.

The second device studied has almost the same characteristics as split A except for t_{si}, which is 20 nm and in this case we have devices without and with GP. These devices refered to as split B in case of no GP, which is the reference device. and split C with GP. All devices were fabricated at imec, Belgium.

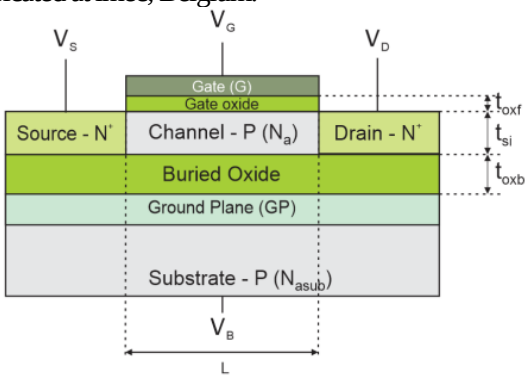

Fig. 1. *A schematic cross-section of an UTBOX/UTBB SOI device with GP.*

The measurements were done with an B1500 Agilent® system. The applied voltage between gate and source (V_{GS}) varied from -2V to 2V for two different drain bias (V_{DS}) values: 50mV (triode) and 1V (saturation).

The extraction of the threshold voltage (V_T) was done based on the second derivative method, which is applied on the I_{DS} as a function of V_{GS} curve [5].

4. Results and Discussion

The first analysis was based on the experimental V_T values shown in Fig. 2, where it is possible to note that when t_{si} is reduced the V_T also reduces. This happens because with a smaller t_{si} the channel depletion region is smaller and there is less charge to invert, so that the voltage needed to invert the channel becomes smaller.

When comparing split B and split C, the device with GP (C) has a higher V_T then the one with no GP (B), what can be explained by the fact that when there is a GP implantation, there is more charge under the buried oxide, since for a device with no GP, the doping concentration is about 10^{15} cm^{-3} and with GP it is about 10^{18} cm^{-3}, making the surface potential at the third interface smaller.

Fig. 3 shows the experimental curve of subthreshold swing (SS) as a function of L. For t_{si}=20 nm the SS value is smaller than for t_{si}=50 nm, this is a consequence from the difference in V_T, since it is smaller, there is less voltage needed to turn on the device and the slope for the curve of

drain current (I_{DS}) as function of gate overdrive voltage (V_{GT}= V_G-V_T) for t_{si}=20 nm is higher than for t_{si}=50 nm, as shown in Fig. 4 for L=1µm and V_{DS}=50 mV.

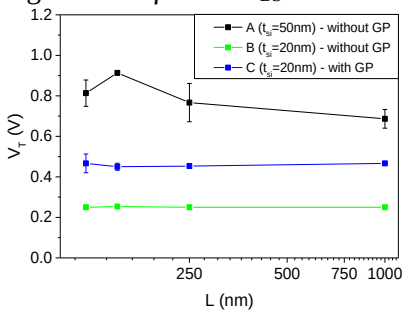

Fig. 2. *Experimental curve of threshold voltage as a function of the channel length.*

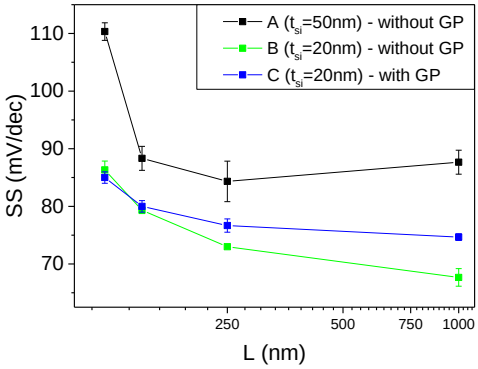

Fig. 3. *Experimental curve of subthreshold swing as a function of the channel length.*

When comparing the splits B and C, the SS values for devices with GP (C) is higher for L=1µm and 250 nm and almost the same for L=150 and 120 nm. For the two largest L, split C has a higher SS due to the higher V_T, but when L becomes smaller the short channel effect (SCE) begins to affect this parameter.

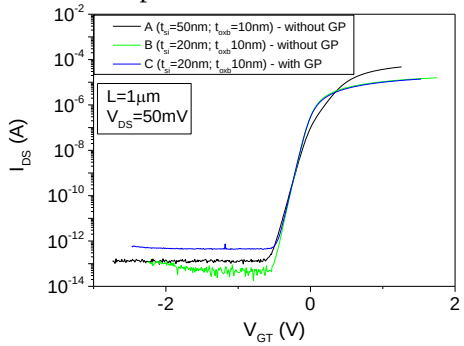

Fig. 4. *Experimental curve of drain current as a function of gate overdrive voltage.*

The DIBL parameter shows the variation of V_T when the device is in triode mode (V_{DS}=50mV) and at saturation (V_{DS}=1V). When comparing a device with t_{si}=20 and 50 nm, the one with 20 nm has less depletion charge at the channel, however, when V_{DS} is increased the potential barrier at the source decreases less than for t_{si}=50 nm, so the V_T variation for t_{si}=20 nm is smaller. The GP does not affect significantly this parameter.

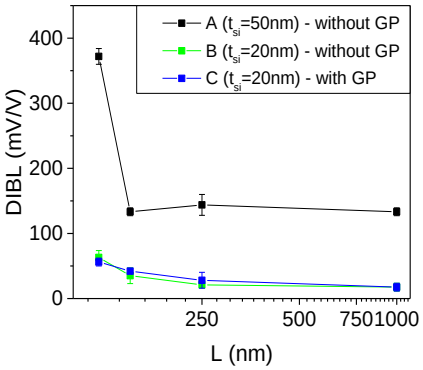

Fig. 5. *Experimental curve of DIBL as a function of channel length.*

5. Conclusion

In this paper the influence of silicon thickness and ground plane implantation were analyzed based on experimental data.

It was verified that when the silicon thickness is reduced, the values of V_T, SS and DIBL decrease. A thinner silicon region results in: a better electrostatic coupling, improving the transistor switch, a small depletion region and consequently, there is less charge to invert reducing the V_T value, and a lower variation of V_T between triode and saturation region, improving the DIBL performance.

With a GP implantation, there is more charge under the buried oxide that interferes at the channel, resulting in a higher values of V_T. During the process of the GP implantation, the trapping of charges at the interfaces (N_{it}) of the transistor can increase. This increase and the better coupling can be the cause for a better SS for the device with GP and t_{si}=20 nm. For devices with L < 250 nm the GP presented a better control of SCE. The GP did not influence the DIBL. With the GP the SCE was better controlled allowing the device downscale without much interference at its performance.

Acknowledgment

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