ZTC Spread Region in Strained and Irradiated nFinFETs

V. M. Nascimento[1]*, P. G. D. Agopian[1,2], E. Simoen[3], C. Claeys[3,4], J. A. Martino[1]
[1] LSI/PSI/USP, University of Sao Paulo, Sao Paulo, Brazil
[2] Sao Paulo State University (UNESP), Sao Joao da Boa Vista, Brazil
[3]imec, Leuven, Belgium, [4] E.E. Dept., KU Leuven, Leuven, Belgium
*email: mesquita@lsi.usp.br

1. Abstract

This paper shows the influence of irradiation and strain on the ZTC (zero temperature coefficient) voltage of SOI nFinFETs. The addition of these effects generates changes in threshold voltage and mobility degradation, which influence the generation of an ZTC area, causing a spreading of it.

2. Introduction

In order to follow the device technological scaling, the electronic components need to be improved to support several harsh environments, and one technology which has shown strong potential for these applications are the SOI FinFETs [1-2].

Due to the small active area and the presence of a buried oxide, this kind of device is good for radiation environments. Its geometry reduces the Single Events Effects (SEE) caused by the radiation particles crossing the transistor's structure. However, the silicon oxide layers (in the gate and buried oxide) are liable to store fixed charges and interface traps causing a big problem for the so-called Total Ionizing Dose (TID) effect since that effect is cumulative in time [3-4].

In order to improve the mobility in FinFET devices, where different channel mobilities between sidewalls and top gate (different crystallography orientation) are present, it is common to implement mechanical strain [5-6].

Therefore, using stress engineering for improving the channel mobility and its employ in harsh environments, the radiation and the strain can cause interface defects, that change the basic physical characteristics.

The ZTC (Zero Temperature Coefficient) point has been used for biasing the circuits to cope with environments with a high temperature variation [7], and is directly dependent on the basic parameters like threshold voltage and mobility. Therefore, interface defects present in the devices need to be investigated to evaluate their influence on the ZTC bias point.

3. Devices Characteristics

The devices used in this work have been fabricated at imec, Belgium. Both non-strained and strained (sSOI) devices containing a selective epitaxial grown (SEG) layer in drain and source are studied. The strained transistors combine the sSOI substrate with a contact etch stop layer (CESL) of SiNx on the gate for optimal stress engineering. A schematic view of the SOI nFinFET device is presented in figure 1.

The devices studied in this work present the following characteristics: channel length (L) of 150 nm, oxide thickness (t_{ox}) of 3 nm with an effective oxide thickness EOT=1.5 nm (the gate dielectric consists of 2 nm HfSiON on 1 nm SiO_2), fin height (H_{fin}) of 65 nm, fin width (W_{fin}) of 20 nm, number of fins (N_{fin}) is 5 with 1 µm of spacing between them and a buried oxide thickness (t_{box}) of 145 nm. More device and process information can be found in ref. [8].

The irradiation was done with a fluency of 10^{12} p/cm^2 without bias and with a proton energy of 60 MeV, that corresponds to an equivalent dose of 100 krad.

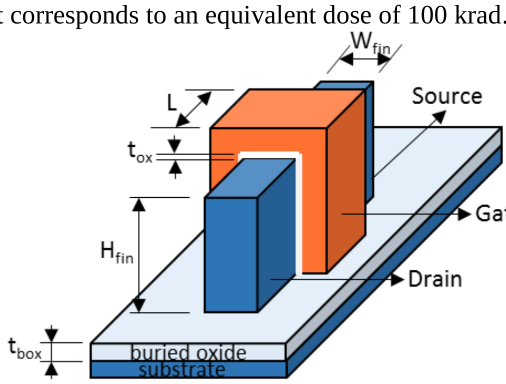

***Fig 1** - A tri-dimensional schematic view of a triple gate SOI FinFET.*

4. Results and Analysis

Figure 2 gives the I_D x V_G curves at different temperatures for a device without radiation and strain effects, showing the cross point called ZTC. The upper part varies due to the mobility degradation with the temperature and the lower part varies because of the increase of the intrinsic carrier concentration with the temperature that reduces the threshold voltage [9].

Figure 3 shows the curves for non-strained and strained devices, and it is possible to notice that the reduction in threshold voltage (V_{TH}) caused by the strain reflects in a reduction of the ZTC voltage (V_{ZTC}), while the interface defects generate a small spread of the ZTC point (cross area of the curves).

Figure 4 shows the comparison between all the devices types (strained, non-strained, irradiated, non-irradiated), and it is possible to notice a small variation of the curves between without and with radiation. Figure 5 (a zoom of figure 4) clearly shows the increase of the ZTC area due to the radiation and consequently the defects caused by it.

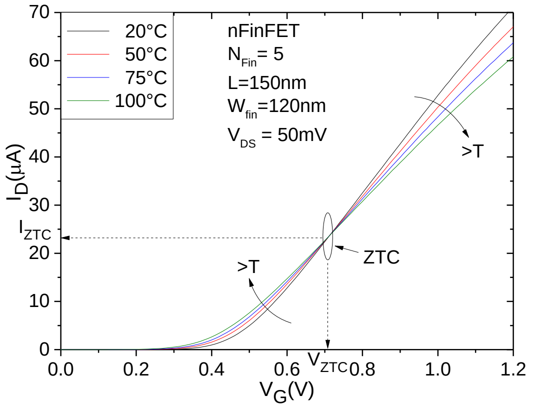

Fig 2 *- Experimental drain current (I_D) in function of gate bias (V_G) for different temperatures for non-strained and non-irradiated devices in the linear region.*

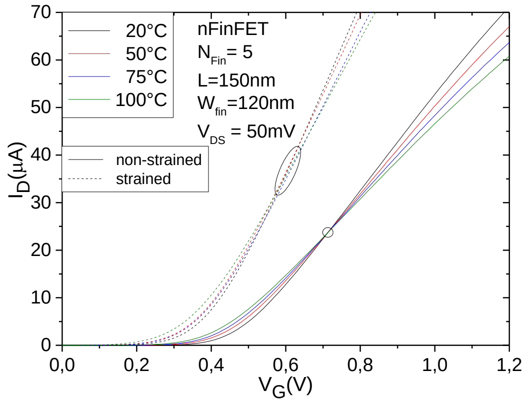

Fig 3 *- Experimental drain current (I_D) in function of gate bias (V_G) for different temperatures for non-strained and strained, non-irradiated devices in the linear region.*

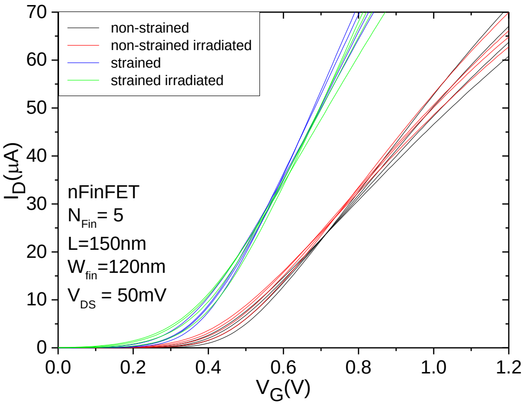

Fig 4 *- Experimental drain current (I_D) in function of gate bias (V_G) for different temperatures for non-strained and strained, non-irradiated and irradiated devices in the linear region.*

It is also possible to observe that the sum of both effects (strain and radiation) causes a higher increase of the ZTC cross-area, due to the sum of the defects in the device's structure, causing a variation in both the threshold voltage and the mobility.

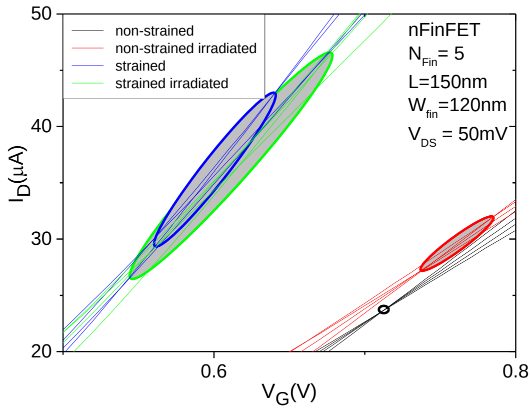

Fig 5 – *Zoom of fig.4 showing the ZTC area.*

5. Conclusions

This work presents an analysis of radiation and strain influence on the Zero Temperature Coefficient voltage for SOI nFinFETs. It was observed that for the studied devices the generated interface defects have an impact on the spread of the ZTC area, resulting in an increase of the area.

Acknowledgments

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