Channel Length Influence on a Self-aligned Triple Gate SOI Tunnel FET

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1. Abstract

In this work, the drain current as a function of gate bias is examined for various channel lengths of triple gate SOI p-TFET devices. The behavior of these transistors is studied for three different channel widths. Finally, the results are analyzed and a comparison is done with other similar characteristics reported in the literature.

2. Introduction

Over the past few years, Internet of Things, mobile communications, wearables and general embedded applications have been pushing the industry needs, introducing new challenges for circuits and devices design. Year after year, better performance and lower power consumption have been becoming fundamental targets that future technologies must achieve.

Process node of 10 nm based on FinFET technology is now being used in mass production for manufacturing new system-on-chip integrated circuits [1]. Even with these advances, the breakdown of Moore's law and Dennard's scaling theory are evidences for the end of the current technology roadmap for semiconductors approaches. New architectures, materials and device structures have been studied for possible replacements in advanced technologies.

In this scenario, the Tunnel Field Effect Transistors (TFET) appear as an alternative device that can offer subthreshold swing values below 60 mV/decade and makes possible to minimize short channel effects, due to its different current mechanism, thereby allowing supply voltage and threshold voltage scaling [2].

The TFET current mechanism is based on injection of carriers from source to channel due to the gate voltage induced band to band tunneling.

Equation (1) describes the tunneling probability, which is directly proportional to the ON current of TFET:

$$T_{BTBT} = exp\left(-\frac{4\lambda\sqrt{2m^*E_g^3}}{3qh(E_g + \Delta\Phi)}\right) \quad (1)$$

Where λ is the tunneling distance, m* is the effective tunneling mass, E_g is the bandgap of the material, q is the elementary charge, h is the Planck constant and ΔΦ is the band bending, in first order analysis, due to the gate bias.

The purpose of this work is to analyze the point p-TFET drain current behavior as a function of gate bias for different channel lengths.

3. Device Characteristics

A simplified diagram of the SOI triple gate p-TFET studied is shown in Fig. 1:

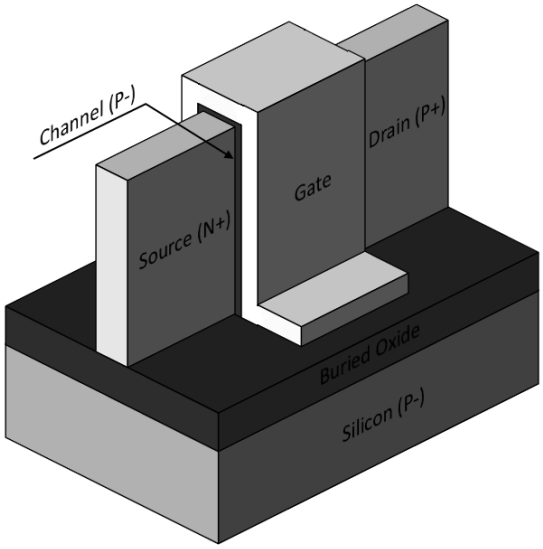

Fig.1. *Self-aligned triple gate SOI p-TFET simplified diagram.*

The studied devices were fabricated on silicon on insulator (SOI) substrates with a 150 nm thick buried oxide. The fin height is 65 nm. The gate stack consists of 5 nm TiN covered by a 100 nm polysilicon layer. The gate oxide is formed by 2 nm HfO_2 on a 1 nm SiO_2 [3].

The conventional structure of TFET devices is a gated PIN diode with self-aligned gate. The channel region was kept with a natural doping, resulting in p-type wafer (10^{15} cm^{-3}). Considering in this work the device as a p-TFET, the N+ region is the source and the P+ region is the drain. The studied transistors have five or fifteen fins in parallel, depending on their width.

4. Analyses and Discussions

As the theory states, the band to band tunneling, whereupon the working principle of TFET devices is grounded, occurs right at the source/channel junction. As it is known, for point TFETs, the channel length does not have a considerable influence on the ON-state drain current, so mainly the gate voltage is responsible for ΔΦ potential drop.

Fig. 2 describes the drain current behavior as a function of gate voltage for lengths from 150 nm to 10

μm in a 40 nm width device, considering -1.5 V of drain to source voltage:

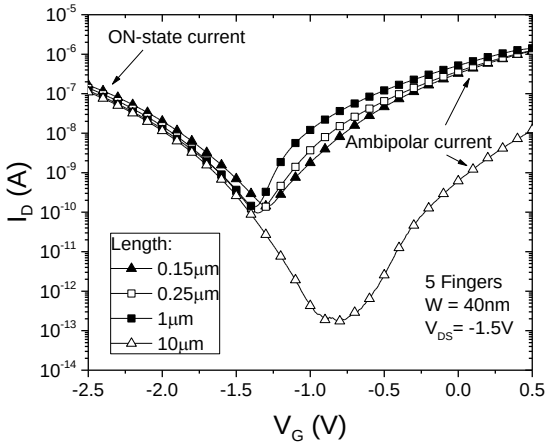

Fig.2. *Drain current as a function of gate voltage for different lengths of 40 nm channel width p-TFET devices.*

As can be observed above, the drain current for devices from 150 nm to 1 μm of channel length are almost the same, just like was expected according to the literature. But, as one can see, the 10 μm length transistor showed a different behavior for both the onset voltage and the ambipolar current. Ambipolarity is a characteristic responsible for the exponential increase of the OFF-state current in a self-aligned gate tunnel FET coming from band to band tunneling that occurs at drain/channel junction under certain bias conditions.

Almost the same behavior was observed for 250 nm wide devices as shown in Fig. 3, also considering -1.5V for drain to source voltage:

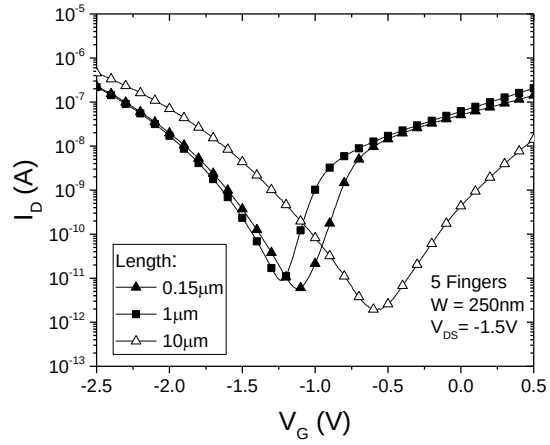

Fig.3. *Drain current as a function of gate voltage for different lengths of 250 nm channel width p-TFET devices.*

This behavior is similar to what is observed in underlap drain/gate region devices used to mitigate the undesirable ambipolar current. As shown in [4], a well-designed underlap between gate and drain can reduce the ambipolarity effect to acceptable levels.

So, based on the observed results it is possible to suggest that a very long channel length (10 μm) introduces a channel resistance equivalent to that introduced by the underlap technique, reducing the OFF-state current and improving the device characteristics for digital applications. This ambipolarity reduction also promotes a minimum I_D shift and consequently an onset voltage shift.

Finally, as one can see in Fig. 4, for such wider devices as 500 nm, the tunneling carrier generation is high enough that the channel resistance increased by longer channel does not affect the drain current behavior.

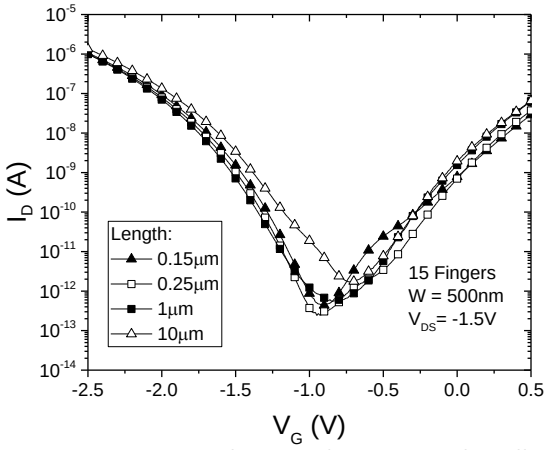

Fig.4. *Drain current as a function of gate voltage for different lengths of 500 nm channel width p-TFET devices.*

5. Conclusion

In this work, the drain current as a function of gate bias was examined for various channel lengths of triple gate SOI p-TFET devices. The behavior of these transistors was observed for three different channel widths. The results suggest that increased channel resistance in 10 μm channel length devices and narrow fin creates a similar effect to what can be observed in transistors with underlap between gate to drain, reducing the OFF-state current and promoting an onset voltage shift.

Acknowledgments

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