Analysis of Self-Heating Effects in Junctionless Nanowire Transistors Through Current Transients

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1. Abstract

This paper presents a study on the influence of temperature dissipation in Junctionless Nanowire Transistors by evaluating self-heating effects in current transients when a pulse is applied to the drain. Different values for channel width and fin height are tested. The analysis is based on three-dimensional simulations.

2. Introduction

The Junctionless Nanowire Transistor (JNT) was proposed as a solution to the difficulties encountered in the process of tri-gate nanowire MOS transistors, such as the creation of abrupt junctions between source/drain and channel, by having a constant uniform doping concentration along the whole silicon region, being no longer necessary source and drain doping of the silicon [1]. These devices also present lower gate capacitances and leakage current, and lower short channel effects have been noticed for lower channel widths [2]. JNTs are generally fabricated using SOI substrates.

However, the low thermal conductance held by the buried oxide silicon results in lower heat dissipation from the device. Temperature raise in the silicon layer is caused by Joule effect due to current flowing through the device. By adding these two issues, a phenomenon can be defined as Self-Heating Effects (SHE) [3].

A list of these effects goes from carrier mobility reduction and consequent current reduction, to negative output conductance, in cases where high power is required. Junctionless devices already show degraded mobility when compared to inversion mode transistors, due to the high doping concentration, which causes impurity scattering in the channel. The raise of device temperature causes scattering mechanisms to help degrading the mobility [4].

Numerous experimental methods are used to understand self-heating through drain current, as described in [5]. Some of them make use of transient analysis of drain current when a pulse is applied. The pulse can both be applied in the drain while the gate is DC biased and in the gate while the drain is DC biased, but the latter may not be suitable for all devices, due to repeated biasing of the gate, which might damage a thin gate oxide.

As opposed to digital circuits, where transistors are biased at a high frequency rate, analog circuits are biased with DC voltage, which makes them susceptible to high temperatures. By applying pulses with time width lower than the time taken for SHE to occur, device characteristics are not changed by the temperature.

In this work, an analysis of the transient and stationary performance is presented for a simulated structure of a JNT with varying dimensions, taking into consideration self-heating effects. The results were obtained by performing 3D simulations on Synopsys Sentaurus Device Simulator [6].

3. Device Characteristics

The simulated structure has a 4-terminal gate structure for thermal contacts on a polysilicon gate material. The device features channel length (L) of 25 nm, channel widths (W) varying from 10 nm to 200 nm and fin height (H_{fin}) varying from 12 nm to 100 nm. The drain and source extensions were removed in order to avoid the series resistance.

The simulations included the thermodynamic model, to account for non-uniform lattice temperature and self-heating effects.

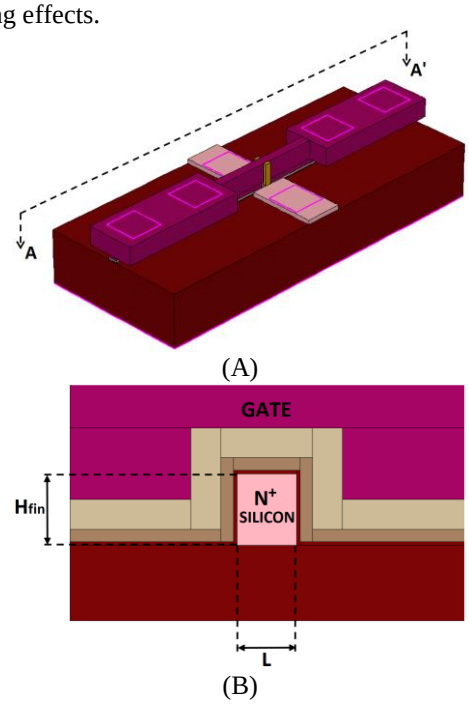

Fig.1. *Three-dimensional scheme (A) and longitudinal (B) section of the simulated device.*

4. Results and Analysis

In order to evaluate at which values of drain biasing the influence of temperature becomes evident in the drain current, it was obtained a series of I_{DS}-V_{DS} curves

varying channel width (W) and fin height (H_{fin}), in addition to the lattice temperature in the center of the channel. An overdrive gate voltage (V_{GT}) of 2 V was set. These curves are presented in Fig. 2.

For smaller devices, the drain biasing did not cause the temperature to rise to values where the drain current would be affected by SHE. As the channel's longitudinal cross section increase, temperature raises for the same applied drain voltage, which causes the current slope to slowly reduce with V_{DS}, presenting at a certain point negative output conductance.

The results show that the 100 nm fin height transistor displays a similar drain current and temperature behaviour than the 200 nm channel width transistor, having half its size. It can also be noticed that fin height scaling has more influence in SHE than channel width scaling, since the current slope is more negative for the same value of these dimensions. This happens because increasing fin height raises current flow more than increasing width, and higher current means heating more the device.

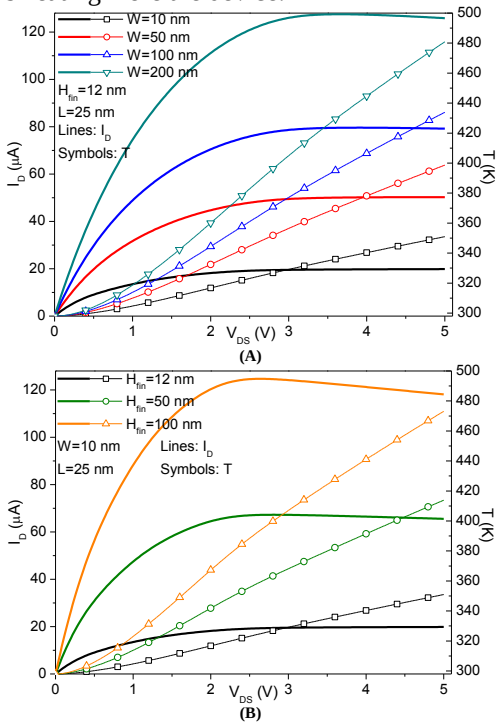

Fig.2. *Drain current and lattice temperature as a function of drain voltage for different channel widths (A) and fin heights (B).*

It was then performed a transient simulation where a 5 V pulse was applied to the drain, while biasing the gate with a V_{GT} of 2 V is obtained, as presented in Fig. 3. It was stated that the self-heating time constant of these devices lies around 30 ns, whereas the high state of the pulse is about 70 ns long, so in all simulations, the presence of self-heating effects is evident. This can also be seen by the fact that even though the drain is only biased for a short time, the devices temperature reached the same temperature as in the I_DxV_{DS} curves.

Comparing the transients for varying channel widths and fin heights, it is possible to see that increasing the

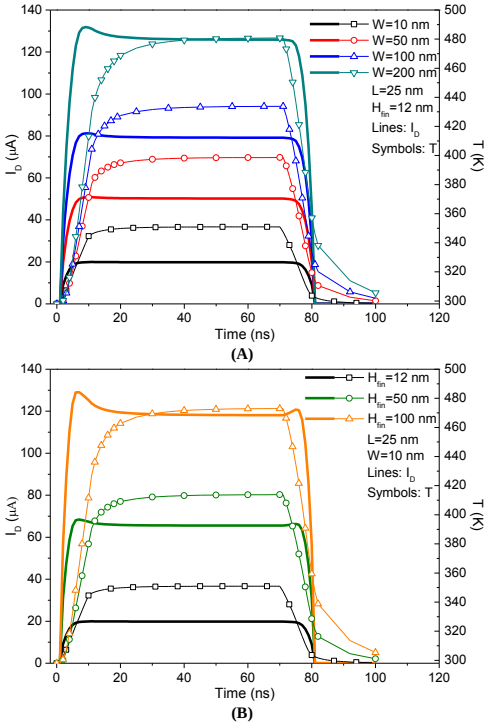

Fig.3. *Drain current and lattice temperature transient for different channel widths (A) and fin heights (B).*

transistor's height implies in higher self-heating effects presented in the drain current as in the DC curves.

5. Conclusions

The simulations showed that increasing fin height makes more impact in self-heating effects than channel width, and that a pulse high state around 10 ns would be necessary to avoid the current to decrease, and 20 ns of low state for the temperature lower back to room temperature, so another pulse can be applied.

Acknowledgments

The authors acknowledge CAPES, CNPq and FAPESP for the financial support.

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