# Field Effect Transistors based on Graphene Micro Channels Defined by Photolithography

A. M. Pascon[1], D. G. Larrude[2] and J. A. Diniz[1,3]

[1] Center for Semiconductors Components and Nanotechnologies, University of Campinas, 13083-870 Campinas, SP, Brazil.

[2] MackGraphe Graphene and Nanomaterials Research Center, Mackenzie Presbyterian University, 01302-907 São Paulo, SP, Brazil.

[3] School of Electrical and Computing Engineering, University of Campinas, 13083-852 Campinas, SP, Brazil.

e-mail: alinepascon@gmail.com

## 1. Abstract

We report an achievement of large area of monolayer graphene produced by chemical vapor deposition process and their implementation into field effect transistors (GraFETs) by pholithography process with definition of ten GraFETs composed by micro wires graphene in the same device, acting as graphene channels.

## 2. Introduction

In the post-silicon era, 2D materials as graphene, composed of sp2 hybrid carbon atoms, emerge as electronic material in the fabrication of field effect transistors, because its outstanding transport properties, flexibility, high electrical conductivity and mechanical strength, since it was first isolated in 2004 by Geim and Novoselov [1]. Today, there are some methods to synthetize graphene, but CVD method ensures higher quality, most efficient in industrial applications, besides lower cost, when compared to other methods to produce large area graphene [2].

Here, we report a device fabrication, applying the photolithography and oxygen plasma etching processes to define the graphene channel region, creating ten GraFETs at the same device parallel connected, corresponding to an increase in transconductance response and consequently increase in carriers mobility.

## 3. Method and Results

*A. Fabrication Process*

The device was fabricated employing 100 nm of titanium and gold (Ti/Au) as contact electrodes deposited by thermal evaporation, followed by deposition of titanium (20 Å) by thermal evaporation, and silicon dioxide (20 nm) by electron cyclotron resonance (ECR) as gate dielectric of the GraFET, as presented in Fig1a. All these regions are defined by liftoff process. The channel was set to a length of 3 µm, while its width will be defined by the graphene micro wires. The monolayer graphene was grown based on the procedure proposed by Ruoff and coworkers on Cu foil [3]. The graphene was transferred to the device using wet transfer method and PMMA as a supporting layer [4].

Figure 1a shows the CVD graphene isolated between the source and drain Ti/Au electrodes, and on the gate dielectric, due the photolithography step followed of the oxygen plasma etching, to remove the graphene in the outside area and define the active region of the device. Figure1b shows the graphene region in details composed of 9 micro structures 0.5 µm wide on average each one, forming 9 GraFETs connected in parallel.

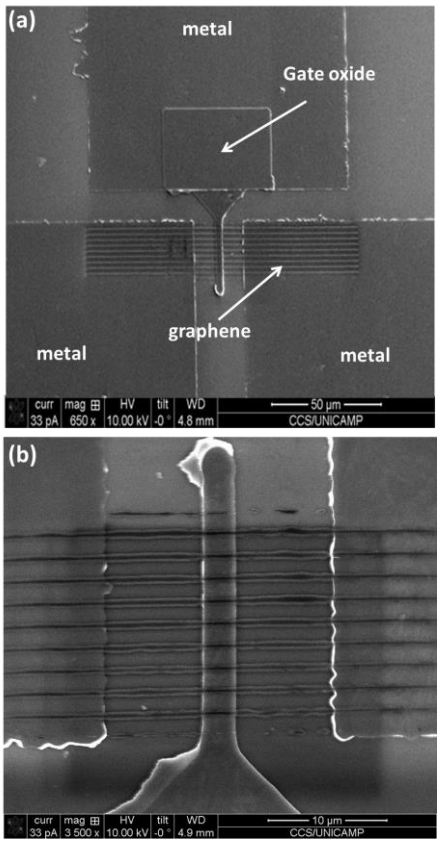


***Fig.1.*** *SEM images of fabricated devices showing graphene region defined by photolithography process. (a) Contact electrodes (metal), gate oxide and monolayer graphene bonding S/D region. (b) Graphene micro channels on gate oxide region in details.*

*B. Electrical Measurements*

Figure 2 shows electrical measurements of the fabricated GraFET. Figure 2a shows $I_{DS}$-$V_{DS}$ characteristics from several values of gate voltage (-3 V $\leq V_G \leq$ +3 V) exhibiting a gate modulation of the transistor, since the current measured between S/D, $I_{DS}$, changes according to voltage applied in the gate for the same voltage applied between S/D, $V_{DS}$. Besides the ohmic behaviour, the curves show that there are no leakage current, due the curves at $V_{DS}$=0 cross $I_{DS}$=0. Total resistance was measured, resulting in 2.3 kΩ. Figure 2b shows the transconductance $g_m$ versus gate voltage $V_G$ measured at $V_{DS}$=0.5 V. Positive and negative transconductance values ($g_m$ = -36.2 µS and $g_m$ = +16.9 µS) indicate the ambipolar behaviour of graphene. These measurements were realized in devices without the annealing process that will be done in the future, to improve the transconductance values and the contact graphene/metal.

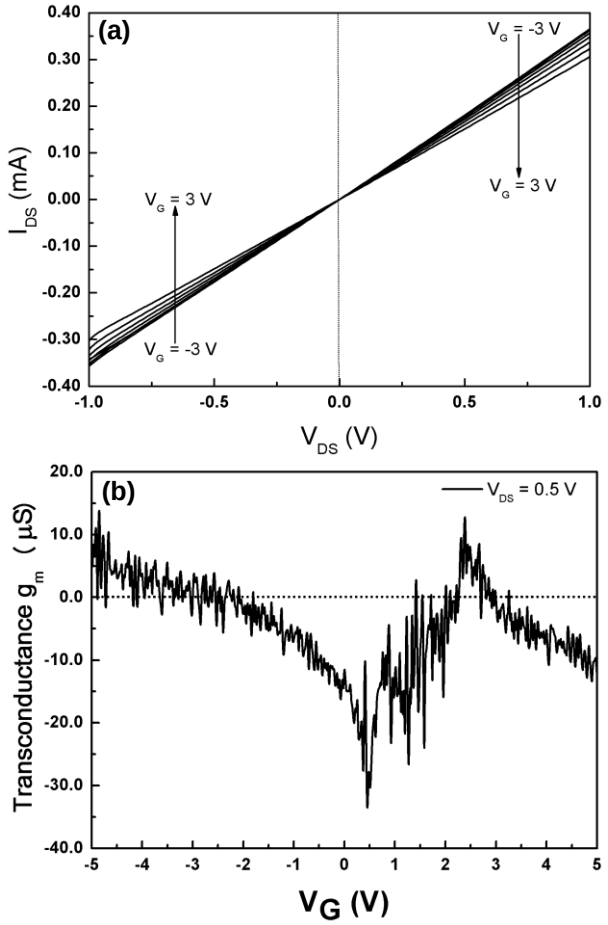


***Fig.2.*** *(a) $I_{DS}$-$V_{DS}$ characteristics from several values of $V_G$ (-3 V $\leq V_G \leq$ +3 V), steps of 1 V and -1 V $\leq V_{DS} \leq$ +1 V for one GraFET.(b)Transconductance $g_m$ vs gate voltage $V_G$ for $V_{DS}$ = 0.5 V.*

## 4. Conclusions

In conclusion, we fabricated a field effect transistor with micro channels of graphene defined by photolithography process, with Ti/Au as contact electrodes and $SiO_2$ as gate oxide. Structural and electrical characterizations were performed showing high definition of the micro channels (0.5 µm wide) that work as 9 GraFETs connected in parallel, and good response to gate voltage bias which should improve applying an annealing process.

## Acknowledgments

This work is financially supported by CAPES and CNPq.

## References

[1] K. S. Novoselov et al., "Electric Field Effect in Atomically Thin Carbon Films", Science 22, Vol. 306, Issue 5696, pp. 666-669, Oct 2004.

[2] X.-D. Chen et al., "High-quality and efficient transfer of large-area graphene films onto different substrates", Carbon, Vol. 56, pp. 271-278, May 2013.

[3] Xuesong Li et al., Science, "Large-Area Synthesis of High-Quality and Uniform Graphene Films on Copper Foils", Vol. 324, 1312-1314, June 2009.

[4] L. Jiao, B. Fan, X. Xian, Z. Wu, J. Zhang, Z. Liu, J. Am. Chem. Soc., "Creation of Nanostructures with Poly(methyl methacrylate)-Mediated Nanotransfer Printing", Vol. 130, 12612-12613, July 2008.