OPTIMIZATION OF AN OTA BY USING A DEDICATED CAD TOOL WITH DIFFERENT HEURISTIC ALGORITHMS OF ARTIFICIAL INTELLIGENCE

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1. Abstract

The analog Complementary Metal-Oxide-Semiconductor (CMOS) integrated circuits (ICs) designs are complex and time consuming tasks because they can be considered as electronic systems with multiple inputs and multiple outputs. Usually, these kinds of systems are solved by using heuristics algorithms of the artificial intelligence. Shuffled Frog Leap Algorithm (SFLA) is capable of designing OTAs with higher tolerance to the variations of the temperature and bias conditions in relation to the Genetic and Imperialist Competitive Algorithms due to it presents a search process that takes into account the local and global searches, simultaneously.

2. Introduction

Currently we have an immense necessity by electronic systems integrated on unique chip. Systems-On-a-Chip (SoCs) usually are composed by sensors, interfaces, memories, microprocessors, and analog integrated circuits [1]. The design cycle time of a SoC is defined mainly by design time of the analog CMOS ICs [1]. This happens because they are fundamentally electronic systems with multiple input variables and multiple output variables [1]. Consequently, the design cycle time is strongly dependent on the expertize of the designer [2]. To overcome this issue, nowadays the analog CMOS ICs designers use commercial optimization computational tools. These computational tools usually incorporate heuristic techniques of the artificial intelligence (AI), which integrate the MOEAs with the SPICE simulator. Recently, it was proposed an in-house optimization computational tool for analog CMOS ICs, entitled MTGSPICE [1], which integrates different MOEAs (Genetic Algorithm, GA [3], Imperialist Competitive Algorithm, ICA [4], and the Shuffled Frog Leap Algorithm, SFLA [2]); all of them are integrated to the Spice Simulator. Therefore, the motivation of this work is to use the different MOEAs of the MTGSPICE to design an OTA and to identify which is the best algorithm that is capable of meeting all specification at the same time.

3. General Description of Heuristic Methods

The GA is based on the Darwin's Law of Evolution by Natural Selection, which the strongest survive. The initial population is generated randomly and is submitted by an evolution process [3]. In the final evolution process, we will have a population with the same number of elements of the initial population, where ideally all elements are able to meet the specifications [3].

The ICA is based on the historical term “Imperialism”. The initial population is composed of "countries”, where there are two types of countries: imperialists and colonies. The term "countries" is like the GA chromosomes [4], which represent the potential solutions obtained by the optimization algorithm. The best countries, defined as Imperialists, are those that are closest to the desired objectives, while the Colonies are those that are most distant from the objectives proposed by the designer [4].

Considering the SFLA, the "frogs" are similar to the ICA countries and each frog is assigned to a subset of a population named memeplex [2]. This strategy allows to combine the benefits of parallel local search processes inside each memeplex, and a global search process by exchanging local information of memeplexes in a shuffling process to perform a global search [2].

4. Single-stage single-end OTA description

The single-stage single-end OTA (Figure 1) [5]: is used in this work because it is a basic analog build block, usually used in several analog CMOS ICs [5].

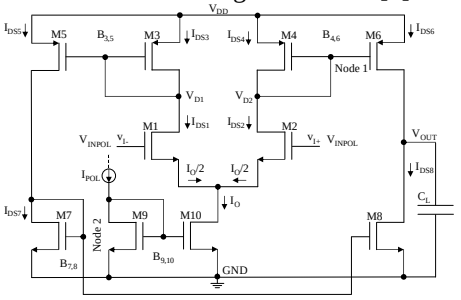

Fig.1. *Schematics of the single-stage single-end OTA used in this work.*

Where C_L is the load capacitance, V_{DD} is the supply voltage, GND is the ground of the circuit, v_{I+} and v_{I-} are the non-inverting and inverting input MOSFET differential pair bias, I_{POL} is the drain current of the MOSFET differential pair, I_O is the output current of OTA, V_{INPOL} is the direct current (DC) gate bias of the MOSFET differential pair [5], I_{DS1} and I_{DS2} are the drain currents of M1 and M2 [5], I_{DS3} and I_{DS4} are the drain currents of the active loads as a current mirror [5], I_{DS5}, I_{DS6}, I_{DS7} and I_{DS8} are the drain currents of the output

stages formed by the transistors M5 and M6 and also by M7 and M8 [5].

5. Experimental Results

The MTGSPICE was used to design an OTA considering the following specifications: technology used was 0.35 μm Bulk CMOS of the ON-Semiconductor and the desired values of the specifications are presented in the "Goals" column of Table I, together with the best results obtained by MTGSPICE regarding the fitness functions values.

***Table I**. Desired specifications and their values obtained by MTGSPICE regarding the best fitness functions values.*

	Goals	**GA**	**ICA**	**SFLA**
A_{V0} (dB)	**≥ 44.0**	44.0	43.1	44.3
f_T (kHz)	**≥ 150.0**	150.0	244.0	158.0
P_{TOT} (μW)	**≤ 5.0**	4.1	5.1	4.7
φ_M (°)	**87.0**	87.8	84.4	87.4
AREA (μm²)	**Minimize**	2750.6	907.7	290.3
f_0 (Hz)	-	935.0	1700.0	966.0
I_{POL} (μA)	-	0.16	0.03	0.36
V_{INPOL} (V)	**0.0**	0.0	0.0	0.0

Where φ_M is the phase margin, A_{VO} is the voltage gain, f_0 is cutoff frequency, f_T is unit voltage gain frequency, the *AREA* is the die area occupied by the OTA, P_{TOT} is the dissipation power, I_{POL} is the current bias of the differential circuit and V_{INPOL} is DC gate bias of MOSFET differential pair.

The following MOEAs were used to design the OTA: GA, ICA, and SFL. The weights of the fitness functions [1] were similar (14.28%) for all MOEAs, the population size was defined as 30, the crossover rate was defined equal to 70%, the mutation rate was considered equal to 3%, the total number of evaluated individuals was defined as 30.000, the total maximum rounds was considered of 30, sigma of the Gaussian curve used to define the profile of the fitness function was of 0.08 (to obtain high precision) [1].

Regarding the 15 best solutions found by the MTGSPICE, which are related to the fitness functions values, Monte Carlo (MC) Analyses were performed for each one to evaluate the different OTA tolerances concerning the variations of the temperature (0ºC-75ºC), operating conditions (V_{DD}: 1.125V-1.375V, and bias current of the MOSFET differential pair: 0.117μA-0.143μA) and manufacturing process (mobility and threshold voltage).

Table II shows the best results obtained by the MC Analyses of the solutions found by MTGSPICE for each MOEA used, which presented the smallest average errors related to the specifications.

We observe based on Table II, that SFLA was capable of designing an OTA, which presented a higher number of specifications more tolerant to the variations of temperature and bias conditions. This can be justified because SFLA is able to perform the local as well as the global, simultaneously.

It is important to note that the solutions shown in Table II are different from the solutions shown in Table I because the best solutions related to the fitness functions do not correspond to the best robustness achieved in the MC analyses [1].

***Table II**. The best results of the MC Analyses, regarding the solutions found by MTGSPICE that presented the smallest errors in relation to the specifications.*

	Goal	**GA**	**ICA**	**SFLA**
A_{V0} (dB)	44	44.4	44.1	44.4
f_T (KHz)	150.0	158.8	152.0	160.2
AREA (μm²)	-	1657.4	4140.0	1083.6
PTOT (μW)	5.0	5.0	4.5	5.0

Table III presents the values of channel length (L) and channel width (W) of the MOSFETs found by the different MOEAs used.

***Table III**. MOSFET Dimensions obtained by the SFLA in terms of lambda (λ =0.35 μm).*

MOSFET	**W (λ)**	**L(λ)**
M1 and M2	144	3
M3 and M4	42	5
M5 and M6	74	5
M7 and M8	5	57
M9	332	4
M10	1231	4

6. Conclusion

Based on the simulations of MTGPSICE and the robustness study through the MC Analyses, it can be verified that the best of the three heuristic techniques is the SFLA. This can be justified mainly due to its search process, which is able to consider both the local and global searches, simultaneously, in contrast to the other MOEAs.

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