Voltage-to-Frequency Converter Design for System-on-Chip Testing in 0.35um CMOS Technology

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1. Abstract

This work presents a temperature-compensated voltage-to-frequency converter (VFC) design in CMOS 0.35µm suitable for system-on-chip testing. The proposed topology uses the multivibrator architecture and allows a rail-to-rail input voltage operation. A simple compensation strategy for the frequency variation with the temperature was included. The VFC operates with 3.3V (+/- 10%) of supply voltage and a temperature range from 0°C to 60°C. The output signal frequency varies between 73.1 kHz to 1.2 MHz depending on the input voltage. Simulation results show a power consumption of 802uW, a relative error below 1.2%, a sensitivity error below 3.42% and a linearity error of 0.03%

2. Introduction

SoC (system-on-a-chip) testing is the testing of system-on-a-chip (SoC) devices. An SoC design is typically implemented block by block and testing is also best done block by block. Experimental tests of on-Chip testing request additional Analog-to-Digital converters which increase the current consumption and area of the chip [1].

A voltage-to-frequency converter (VFC) offers a solution for the analog-to-digital conversion, its area is smaller [2] and its power consumption is lower than an ADC [3], besides a VFC can be directly interfaced to a microcontroller using a single digital input/output port. It is necessary a frequency-to-code conversion in the microcontroller for getting done the analog-to-digital conversion [4].

This work presents the design of a voltage-to-frequency converter for system-on-chip testing in 0.35µm CMOS technology. This design presents low power consumption, high linearity, and a rail-to-rail input voltage. Section 3 presents briefly the designed VFC architectures. Section 4 describes the VFC design and presents simulations results. Finally, the conclusions are presented in section 5.

3. VFC architecture

The proposed VFC architecture is presented in Figure 1. The VIC (Voltage-to-current converter) block convert the input voltage (Vin) to current,

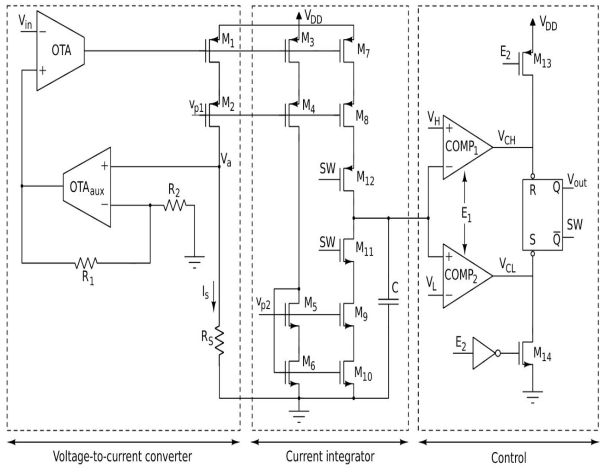

Figure 1. Proposed voltage-to-frequency converter topology.

following this, the VIC output current is integrated by a capacitor, whose output voltage is a linear triangular wave between two voltage levels V_H and V_L. The control circuit drives the current integrator and establishes a square a voltage signal with frequency directly proportional to the input voltage (Fo = K·Vin).

The VIC block is based on a negative feedback composed of two operational transconductance amplifier (OTA and OTAaux), M1 and M2 transistors and Rs, R1 and R2 resistors as shown in Figure 1. The input voltage (Vin) is scaled by a factor $\alpha=R2/(R1 + R2)$ at node Va ($Va= \alpha Vin$) which increase the input dynamic range contrasting with the traditional topology. In the tradition topology (without OTAaux) The input Vin must be sufficiently low to keep M1 and M2 in saturation. OTAaux and the R1-R2 feedback network permit to relax the Vin requirement for M1 and M2 saturation. To obtain a rail-to-rail circuit operation the input OTA was designed with a rail-to-rail topology. This OTA is composed of two differential pairs, a PMOS and other NMOS pair. Furthermore, a symmetric topology with PMOS differential pair was used to implement the auxiliary OTA. The current integrator copies the current established by the VIC using a high-swing cascode mirror, in order to improve the current copy and manage low voltages [5]. The current integrator includes the M11 and M12 transistors operating as switches which defines the capacitor current flow. The

control circuit is constituted by two comparators and a RS flip-flop as shown in Figure 1. This circuit turns-off or turns-on the M11 and M12 transistors controlling the Capacitor charging/discharging. The waveform of the capacitor voltage (Vcap) is a linear triangular signal between the V_H and V_L references voltages. The flip-flop output signal (Vout) correspond to a square signal with frequency proportional to the input voltage (Vin). Figure 2 shows the waveforms of the main signals of the VFC circuit operation.

4. Circuit Design and Results

This equation that describes the relationship between the output frequency (Fout) and the design parameters of this architecture is given by:

$$Fout = \frac{aV_{in}}{2KC(V_H - V_L)R_s}$$

Where S is the scale factor of the voltage Vin, which is defined as S = R1/(R1 + R2), K is the scale factor of the current mirrors, C is the integration capacitor, V_H and V_L are the voltage reference voltages and Rs is the voltage-to-current resistor. For the proposed design R1 = R2 was selected which correspond to ɑ=0.5, which help to keep M1 and M2 in saturation. Rs was set to 20 kΩ and C to 3.2 pF as a trade-off between current consumption and area. The current mirrors scale factor was set to 8 in order to reduce power consumption. In order to reduce the impact of temperature variations and optimize area [6], Rs is formed as a series connection between a RPOLYH material resistor (TC=-0.4x10^{-3}K^{-1}) and other RNWELL resistor (TC=6.2x10^{-3}K^{-1}). M11 and M12 transistors operate like switches in the current integrator, those transistors were designed using the minimum channel length, likewise, RS flip-flop and the comparator transistors. The above setting was performed in order to obtain the speed requirement.

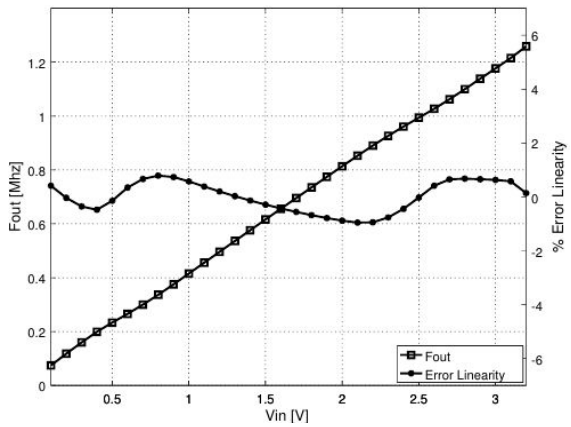

Figure 2. VFC Output frequency and the linearity error as function of the input voltage.

Figure 2 shows the VFC Output frequency and the linearity error as function of the input voltage. output frequency has a mean relative error less than 1.2 % and the sensitive error is 3.4 %. The designed VFC specifications are compared with other works in Table 1, where a compatible linearity error value is obtained for a rail-to-rail operation presented in this work .

Parameter	Ref. [7], 2009	Ref. [8],2011	This Work
Technology	0.35 μm	0.18 μm	0.35 μm
Supply Voltage	3.0 V	1.8 V	3.3 V
Sensitivity	1 MHz/V	1.23 MHz/V	381.04 kHz/V
Input Voltage Range	1.0 V 2.0 V	0.1 - 1.6 V	0.1 V - 3.2 V
Fmin	1.2 MHz	0.122 MHz	0.074 MHz
Fmax	2.2 MHz	1.98 MHz	1.25 MHz
Relative Error	< 0.7 %	< 4.8 %	< 1.2%
Linearity Error[2]	–	0.017 %	0.03 %
Power Consumption	1.03 mW	0.423 mW	0.802 mW

Table 1. VFC specifications compared with others works.

5. Conclusions

A compact 3.3V 0.35um CMOS voltage-to-frequency converter with a rail-to-rail input stage and a temperature-compensated technique was designed. Circuit such as a RS flip-flop, comparators, high-swing cascode current mirror, symmetrical OTA and rail-to-rail OTA make out of this VFC. It's output signal frequency range is 74.39 kHz to 1.2 MHz and it presents a low power consumption compared with other works showing a good performance considering Monte Carlo and Corners simulations.

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