Tridimensional Numerical Simulation and Electrical Characterization of Stacked Nanowires SOI MOSFETs

B. C. Paz[1] and M. A. Pavanello[1]
[1] Department of Electrical Engineering, Centro Univeritário FEI, São Bernardo do Capo, Brazil
e-mail: bcpaz@fei.edu.br

1. Abstract

The aim of this work is to present an analysis of the basic electrical parameters of vertically stacked p-MOSFET nanowires (NWs). The evaluation is carried out through tridimensional numerical simulations and also experimental measurements. The electrostatic potential, transfer characteristics, threshold voltage (V_{TH}), subthreshold slope (S) and effective oxide thickness (EOT) are the main figures of merit.

2. Introduction

Nanowires MOSFETs are one of the most promising devices for future technological nodes that would allow the continuity of the CMOS roadmap. Due to better electrostatic control of the charges in the channel region, multiple gate architecture leads to significant reduction of the short channel effects comparing to planar MOSFETs [1], [2].

In order to reach higher on-state drain current levels and comply with ITRS (International Technology Roadmap for Semiconductors) requests, additional technologies have been developed to boost MOSFETs performance, such as the use of mechanical stress, different materials and channel orientation [3]–[5]. Recently, high selectivity etching process of Si/SiGe multilayers contributed to the development of a new sophisticated structure, called vertically stacked nanowires [6]. Such devices enhance the overall drive current (I_{DS}) once they present larger effective channel width (W_{eff}), where W_{eff} is approximately proportional to the number of beams.

In this work, advanced stacked NWs are analyzed considering different fin width (W_{FIN}) and channel length (L). Simulated results for the electrostatic potential, drain current (I_{DS}), V_{TH} and S are presented. EOT is extracted by fitting C-V experimental measurements to modelled curves.

3. Tridimensional Numerical Simulations Results

The studied transistors are undoped p-type Si nanowires, with two levels staked wires. Silicon thickness (H_{FIN}) is equal to 10nm and W_{FIN} is equal to 15nm and 30nm. The geometrical parameters W_{FIN} and H_{FIN} are the same for both top and bottom wires. The buried oxide thickness (BOX) is 145nm and the L varies from 100nm down to 10nm. The characteristics of the transistors have been simulated in order to reproduce the physical devices fabricated in [7].

Sentaurus Device Simulator, from Synopsys, has been chosen to perform all the tridimensional numerical simulations [8].

Fig. 1 shows the simulated structures in details. All the internal lines of the tridimensional stacked NW are presented in (a), the overall perspective in (b), the longitudinal section, along L, in (c) and the cross-section, along W_{eff}, in (d). It is possible to observe that the bottom wire has Ω shape, while the top wire is Gate-All-Around (GAA).

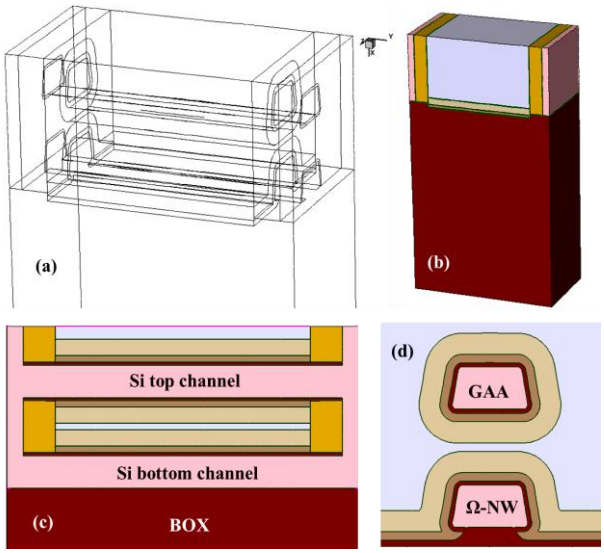

Fig.1. *Simulated stacked NW perspectives (a) and (b), longitudinal section (c) and cross-section (d).*

From Fig. 2, through the distribution of the electrostatic potential along the NW cross-section, it is possible to note that the Ω-shaped bottom wire induces significant gate control in the bottom surface channel, especially for narrow transistors (W_{FIN} = 15nm), whose behavior is closer to GAA devices.

Fig. 3 presents I_{DS} as a function of the gate voltage (V_{GS}) for p-NWs with W_{FIN} = 15nm and 30nm (a), V_{TH} and S as a function of L for W_{FIN} = 15nm, at low drain bias (V_{DS} = -40mV). It is observed reduced short channel effects because of strong gate control, as expected due to the sum of the Ω and GAA shapes. Assuming degradations of up to 10% for both V_{TH} and S, the stacked p-NWs with W_{FIN} = 15nm keep excellent performance down to channel length of 30nm.

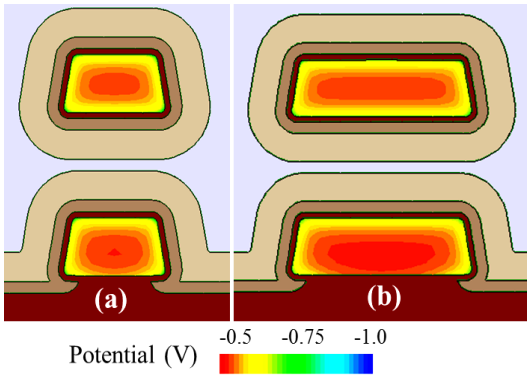

Fig.2. *Electrostatic potential distribution along the fin width for stacked p-NWs with W_{FIN} = 15nm (b) and 30nm (a), V_{DS} = -40mV and V_{GS} = -1.5V.*

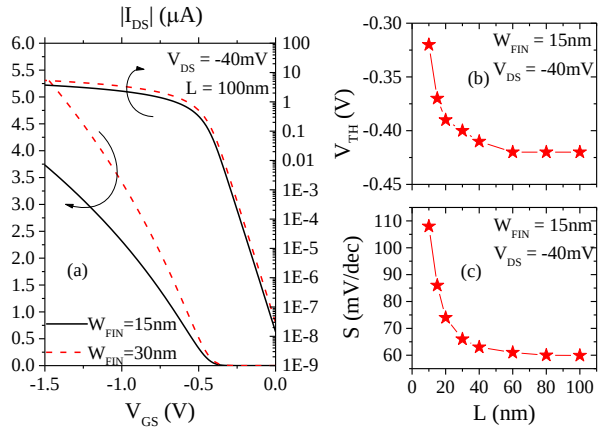

Fig.3. *I_{DS} as a function of V_{GS} (a), V_{TH} (b) and S (c) as a function of L for different p-NWs MOSFETs, V_{DS} = -40mV.*

4. EOT Extraction

Vertically stacked p-NWs MOSFETs have been recently fabricated [7], using replacement metal gate (RMG) process and gate stack composed by HfO_2/TiN/W. EOT characterization is then crucial to allow further investigations of this new technology.

Once there are differences between the top and bottom wire and significant imprecisions on determining the real W_{eff} of experimental NWs, (1) was used to calculate the measured gate to channel capacitance per unit of area (C_{GC}), without using W_{eff}.

$$C_{GC} = (C_{GC,2} - C_{GC,1}) / 3 \times \Delta W \times L \quad (1)$$

$C_{GC,2}$ and $C_{GC,1}$ are the gate capacitance of two stacked NWs with different fin width masks ($W_{FIN,1}$ = 15nm and $W_{FIN,2}$ = 65nm) and ΔW is the difference between the masks, $W_{FIN,1} - W_{FIN,2}$ = 50nm, which consists in a more reliable parameter than $W_{FIN,1}$ and $W_{FIN,2}$, usually different from the real fin width values.

The experimental results have been fitted to the modelled curves resulted from solutions obtained by Poisson-Schrödinger solver. Fig. 4 presents C_{GC} as a function of V_{GS} for p-NWs with L = 100nm, where can be observed the extracted EOT around 1.1~1.2nm.

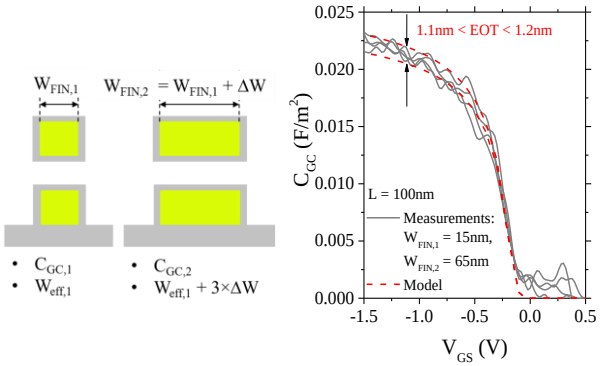

Fig.4. *C_{GC} versus V_{GS} for measurements and model.*

5. Conclusions

The short channel effects have been evaluated, through V_{TH} and S, for p-type vertically stacked NWs through tridimensional numerical simulations. The results show excellent performance and great scalability down to L = 30nm. Electrostatic potential distribution along W_{FIN} demonstrates that the bottom Ω-shaped wire behaves similarly to the top GAA wire, promoting high gate control over the charges in the channel.

Model fitting allowed EOT extraction from experimental measurements of stacked NWs fabricated with RMG process and complex gate stack.

Acknowledgments

The authors would like to acknowledge CAPES, CNPq and São Paulo Research Foundation (FAPESP) grants 2015/10491-7 and 2016/06301-0 for the financial support and CEA-Leti for supplying the devices, which were fabricated under the NANO 2017 program and SUPERAID7 (grant N°688101) project.

References

[1] J.-P. Colinge, "Multiple-gate SOI MOSFETs," *Solid-State Electronics*, vol. 48, no. 6, p. 897–905, 2004.

[2] S. Barraud *et al.*, "Performance of Omega-Shaped-Gate Silicon Nanowire MOSFET With Diameter Down to 8 nm," *IEEE Electron Device Letters*, 33, 11, p. 1526–1528, 2012.

[3] R. Coquand *et al.*, "Strain-Induced Performance Enhancement of Trigate and Omega-Gate Nanowire FETs Scaled Down to 10-nm Width," *IEEE Transactions on Electron Devices*, 60, 2, p. 727–732, 2013.

[4] M. O. Baykan, S. E. Thompson, and T. Nishida, "Size- and Orientation-Dependent Strain Effects on Ballistic Si p-Type Nanowire Field-Effect Transistors," *IEEE Transactions on Nanotechnology*, 11, 6, p. 1231–1238, 2012.

[5] M. Casse *et al.*, "Study of piezoresistive properties of advanced CMOS transistors: Thin film SOI, SiGe/SOI, unstrained and strained Tri-Gate Nanowires," in *IEDM*, 2012.

[6] T. Ernst *et al.*, "Novel 3D integration process for highly scalable Nano-Beam stacked-channels GAA (NBG) FinFETs with HfO2/TiN gate stack," in *IEDM*, 2006.

[7] S. Barraud *et al.*, "Vertically stacked-NanoWires MOSFETs in a replacement metal gate process with inner spacer and SiGe source/drain," in *IEDM*, 2016.

[8] "Sentaurus Device User Guide." Synopsys, 2009.