Logic Inverter SOI MOSFET Operating at High Temperature

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Abstract

This study uses analytical models to demonstrate that behavior of an inversion voltage and the current flowing through the logic inverter are extremely sensitive and dependent on the size of the transistors which forms the circuit and the temperature at wich they operate.

Two-dimensional numerical simulations were performed using ATLAS simulator studying a SOI MOSFET logic inverter, changing the channel length relationships L_p and L_n, which are the lengths of the transistor channels PMOSs and NMOS respectively.

The static voltage curve depending on the temperature ($V_{in}\ x\ T$) and current curves ($I_{DS}\ x\ V_{in}$) with the temperature changing from 27ºC to 300ºC.

1. Introduction

SOI MOSFET technology has several advantages over a conventional CMOS transistor, such as lower threshold voltage variation as the temperature increases [1]. Also it has better performance under critical conditions for example in high external temperatures or exposure to radiation [2]. As these devices suffer a reduction in their dimensions due to the technological advance, efficient heat dissipation is a more recurrent problem. These devices are widely used in the industry, such as the automotive industry [3,4], internal electronic control of Automotive engines [5], aerospace applications, nuclear applications [6], ABS brakes, electronic injection and boilers [2,6].

2. Analysis of the inversion voltage (V_{INV}) of a logic inverter according to the temperature variation

The inversion voltage of the logic inverter is directly related to the β, wich follows the equation:

$$V_{INV} = (2 + \sqrt{\beta})/(1 + \sqrt{\beta}) \qquad (1)$$

For all simulations it where used two-dimensional simulations where useds, so $W_p = W_n = 1\ \mu m$, wich are channel widths of the transistors PMOS and NMOS, respectively. Transistor NMOS channel doping $5x10^{18}\ cm^{-3}$ and PMOS $5x10^{16}\ cm^{-3}$. Drain and source doping $1x10^{20}\ cm^{-3}$. Therefore, the only changed parameters were the lengths of the channels of the transistors PMOS and NMOS, called L_p and L_n.

$$\beta = \beta_n/\beta_p \qquad (2)$$

The results of the simulations are described in the Fig.1 with the parameter varying $1/4 \leq \beta \leq 3$ and operation temperature of 27ºC to 300ºC.

The results are described in Fig.1 where it can be concluded that for $\beta > \frac{1}{2}$ the voltage (V_{INV}) decreases as the temperature increases. Values lower than $\beta < \frac{1}{2}$, V_{INV} increases as it increases the temperature.

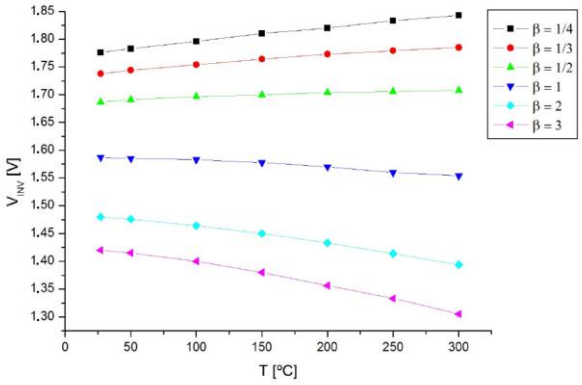

***Fig.1**: $V_{INV}\ x\ T$ curve to $\frac{1}{4} \leq \beta \leq 3$.*

Considering $\beta = 1/2$, V_{INV} practically does not changes with increasing temperature.

Therefore, it can be conclude that a more reliable SOI MOSFET logic inverter is less susceptible to temperature variation when $\beta = L_p/L_n = 1/2$.

3. Behavior of the inversion current as a function of the temperature

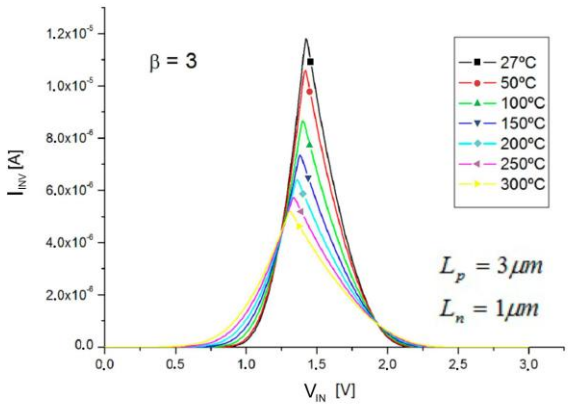

***Fig.2**: $I_{INV}\ x\ V_{IN}$ curves of a SOI MOSFET logic inverter operating from 27°C to 300ºC with $\beta = 3$.*

As presented in Fig. 2, it can be seen the behavior of the current curve $(I_{INV}\ x\ V_{IN})$ as the temperature increases. As the temperature increases, regardless of the value of β, the current I_{DS} always decreases. Equation 3 proves this behavior.

$$I_{DS} = \frac{1}{2}\mu . C_{ox} . \frac{W}{L} . (V_{GS} - V_{th})^2 \qquad (3)$$

Independently of the transistor applied in the equation (3) the current flowing in NMOS and PMOS transistors decreases with increasing temperature because of the fall in mobility(μ).

Just as a comparison, L_p it will be used in the abscissa axis, since the ratio $\beta = L_p/L_n$ is constant.

Figure 3 shows that the ratio $\beta = L_p/L_n$, if it is constant, the result is always a reduction on the maximum current (I_{max}), flowing through the inverter. However, the higher is the L_p values, lower it will be its variation (3), when temperature increases, as it is demonstrated in Fig.3.

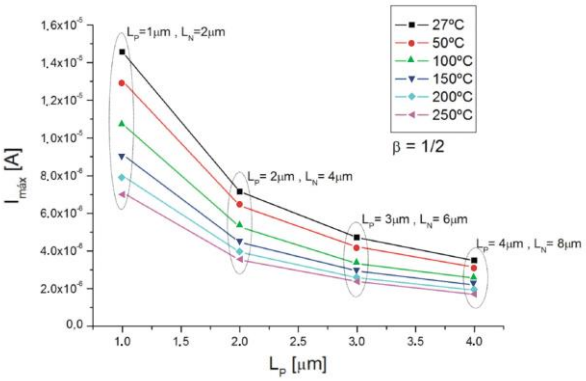

***Fig.3**: Curve $I_{max}\ x\ L_p$ of a SOI MOSFET logic inverter operating from 27ºC to 300ºC.*

The β parameter is also a key factor on maximum current that flows through the inverter, confirmed by equation (3). So, the current I_{DS} is inversely proportional to the channel length of the Nmos and pMOS transistors, even when the devices are submitted to high temperatures.

Fig.4 shows that when $\beta = 1$, regardless of temperature, the largest possible I_{INV} current is flowing through the inverter. Therefore, for β = 1, the current imposes a "mathematical domain" of the current and indicates the maximum values in which I_{INV} can achieve. Any relation to $\beta \neq 1$ causes I_{INV} to be limited in its interior. These results are observed for the other temperature values between 27°C to 300°C, obtaining the same results.

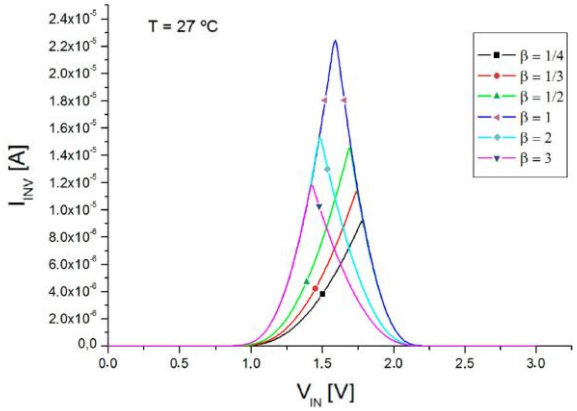

***Fig.4**: Curve $I_{INV}\ x\ V_{IN}$ of a SOI MOSFET logic inverter operating at 27ºC with $\frac{1}{4} \leq \beta \leq 3$.*

4. Conclusions

The present results show the behavior of the current and voltage of a SOI MOSFET logic inverter operating from 27 to 300ºC. It is concluded that the temperature and the dimensions of the transistors are fundamental and determinant factors in the operation of the circuit.

Regarding to the current flowing through the inverter, it was concluded that β is a fundamental factor in the device behavior, and it is proved that the lower it's the β value, higher the current flow through the inverter is going to be. It has also been concluded that the current is maximal at lower values L_P and L_N for a ratio of β = 1.

Acknowledgments

I would like to thank Professor Marcello Bellodi for his support in writing this article.

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