Flip Chip Technology using Gold Stud Bumps

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1. Abstract

Gold (Au) stud bumps were fabricated using a modified wire bonding process. With gold stud bumping, unlike other chip bumping processes such as solder deposition, the chip does not require preprocessing such as Under Bump Metallization (UBM). To complete the interconnection, the chip was bonded onto a gold covered substrate using a thermocompression/sonic process.

2. Introdution

Flip Chip technology is expected to reach $25 billion market value and wafer demand of 32 million (12"eq.wafers) in 2020. Flip Chip solutions have been largely adopted towards the mobile-wireless, consumer and computing applications, including continuous growth in the LED and CMOS Image Sensor (CIS) segments. That growth will be led by Moore's law pushing beyond the 28nm node and 'More than Moore' evolution in next generation DDR and 3DICs [1].

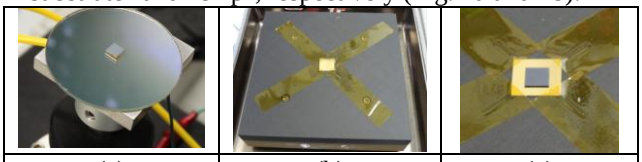
Flip Chip is a form of electronic packaging introduced by IBM in the early 1960s where the chip is mounted directly "upside down" on the substrate. Also called or Controlled Collapse Chip Connection (C4) it was only used in very specific applications where high integration of level 1 interconnects was required. Currently, this technology is used as substitute for encapsulated chips and CoB due to the large volume reduction provided, which can reach 95% because it eliminates the area occupied by wire bonds and capsules used in conventional packaging. Other advantages are high chip performance because delays are avoided due to parasitics caused by the large amount of wire bonds, higher input/output density since Flip Chip allows the use of the whole area of the die, mechanical resistance and low cost for large production volumes. Another advantage of Flip Chip with Au stud bumps compared to conventional solder balls (SnPb, SnAgCu, etc ...) is that it does not require UBM layer processing [2] and can be used directly on Al and Au pads at die level, which facilitates its implementation and is more appropriate to the type of service normally requested by the Electronic Packaging Research Group (Núcleo de Empacotamento Eletrônico – NEE) at CTI Renato Archer. This type of technology using the thermocompression/sonic process allows lower temperatures to be used in the welding process, which reduces the stress to which the chip/substrate assembly is subjected, what is a great advantage from the point of view of product durability. Since the chip and substrate are constructed of different materials, they therefore have different coefficients of thermal expansion (CTE). The use of high temperatures for welding would lead to a large difference in the dilation of these different materials, which translates into stress accumulated at the connection points and interfaces, i.e., at the welding points, leading to early failure. By reducing the temperature through the thermosonic process, we reduce stress levels and, therefore, increase the durability of the assembled system. Moreover, bonding force can be much lower compared to thermocompression bonding, resulting in less mechanical stress to substrate and component which is advantageous if materials are susceptible to deformation or cracking [3].

Au stud bumps are typically used for applications that require a finer pitch than solder bump technology. These finer pitches enable greater functionality to be integrated onto a chip while maintaining a small form factor. A mainstream application of gold stud bumps is for surface acoustic wave (SAW) filters used in mobile phones and other radio frequency (RF) applications. Additionally, many devices, including biomedicals, microelectromechanical systems (MEMS) and optoelectronics require the surface of the active area to remain free from flux or other residues typically used in the solder bumping process to attach the device to a substrate. Au stud bumps do not require flux [4].

The Au stud bumps proposed in this project is one of the ways to interconnect the chip inverted to the substrate ("flip"), while providing mechanical attachment and electrical connection between the two elements, chip and substrate.

3. Experimental Procedure

2" <100> Oxidized Si wafers were coated with 30nm Ti and 200nm Au by Sputtering and cut into 100x100mm and 50x50mm squares to simulate "substrate" and "chip", respectively (Fig. 1a and 1b).



(a)	(b)	(c)

Fig. 1. *(a) Chip on the Pick up Stage, (b) Substrate on the Work Stage, (c) Chip flipped and bonded onto the substrate*

Four Au stud bumps were made on the chips using a modified wire bonding process. The chip was then "flipped" (Fig. 3c) onto the "substrate" using the Eagle 860 Omni Bonder (Semiconductor Equipment Corp.) equipment (Fig. 2) and the thermocompression/sonic process.

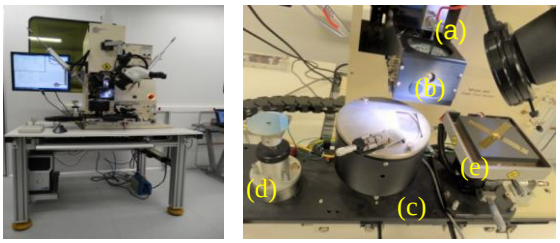


Fig. 2. *Eagle 860 Omni Bonder equipment and some details of it.*

Details of the Eagle 860 Omni Bonder are shown on Fig 2, where: (a) Vertically adjustable head supporting the chip; (b) Optical arm that provides the image of the chip in the above support and the substrate in the Work Stage, to precisely align the two, chip and substrate - this arm is retractable, being collected after alignment; (c) It is the adjustable base in the XY positions where the Pick up Stage (d) and the Work Stage (e) are placed.

4. Results and Discussion

The flip chip process using the Eagle 860 Omni Bonder equipment covers several steps. Firstly, the machine needs to be configured to the ultrasonic process, which means that the Ultrasonic Head must be installed. An specific tool is used for each die size, so the head must also be tuned for the tool in use. Substrate and chip stages must be properly aligned to avoid the tool crashing onto the parts to be bonded and several vertical movements of the Ultrasonic Head (e.g. die search position, focus position,...) need to be configured for the various working positions. Only then the bonding parameters are set on the equipment and on the ultrasonic generator.

Bonding parameters are stored as a "Macro" on the controlling software and contains several bonding steps, as “pick up” of the chip and "place and bond" of the chip in the substrate and can be very complex, including heating ramps and even other macros inside.

The Ultrasonic time and power conditions are set apart in the ultrasonic generator, which can operate in two different modes, defined as Servo and Mode2. In Servo mode, the ultrasound application starts when a pre-defined minimum load is reached by the load cell, while in Mode 2 the ultrasound application starts after the total bond load is reached by the load cell.

Initial welding tests were done using basic parameters found in the literature [3] [5] and also in the work developed during the fellowship CNPq #313201/2015-3. Table 1 below shows the initial parameters that are being used for process development. The Eagle 860 Omni Bonder has also other features such as hot gas, rapid heating/cooling and macro chains that will be evaluated on further opportunities.

Table 1. *Initial parameters for Flip Chip using Au stud bumps on the Eagle 860 Omni Bonder equipment*

ULTRASONIC PARAMETERS (SERVO MODE)			MACRO PARAMETERS			
START LOAD (g)	ULTRASONIC TIME (ms)	ULTRASONIC POWER (EU)	STAGE TEMPERATURE (° C)	PICK LOAD (g)	BOND LOAD (g)	BOND TIME (s)
160	1000	1500	120	10	200	2

Next steps include tests to define the process for Au stud bumps Flip Chip in a reproductive way for the present test vehicle and evaluate the load (force) required as a function of the bump array dimensions and geometry.

Initial inspections will be conducted on X-ray analysis to look for non-bonded areas and, cross section to evaluate the high loss of the bumps due to the Flip Chip process. The results will allow a fine tuning of the Flip Chip process. Subsequently, the assemblies will be scaled to more complex geometries such as daisy chains and interconnect arrays for electrical characterization. The final test vehicle will be to assemble actual and functional devices on a dedicated substrate, comparing electrical parameters and other figures-of-merit before and after the Flip Chip is done.

5. Conclusions

In this paper we showed the Eagle 860 Omni Bonder operation with the Ultrasonic Head. Five (5) instructions manuals were created to describe the equipment use. The Flip chip technology is now available at NEE/CTI and the functional recipe will be studied for process optimization.

Acknowledgments

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