Verification Challenges in Analog-Digital Interfaces

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1. Abstract

The steady advancement of IC technology has led to the fabrication of complex circuits composed by digital, mixed signal (AMS), and radiofrequency (RF) parts. The correct matching between the different domains is required in order to maintain the functionality of the design. Particularly, the interface between digital and analog blocks represents potential source of errors; the digital-analog interaction must be considered in a design verification process and needs to be carefully checked.

Keywords - Analog-Digital Interface, Verification Process, Interface Verification.

2. Introduction

As result of the steady advancement of IC technology, more complex integrated circuits are being developed nowadays, composed by digital, analog and mixed signal (AMS) and radiofrequency (RF) parts, with high performance and reliability. Most of the designs are composed by blocks, or Intellectual Property (IP), that come from different vendors.

The verification process is responsible for ensuring that the design behaves like it was defined in the specification. According to [1], the verification process represents between 60% and 70% of the time and resources spent in the IC development.

The process of integrating digital and analog components in the same die requires the correct matching between them; otherwise, malfunctions may occur. This mismatch may not be noticed at the design integration phase, therefore, errors are not commonly detected before manufactured.

Currently, the interaction between digital and analog blocks within complex systems has increased drastically, requiring a mixed-signal circuit verification approach that may treat these domains together, detecting anomalies on their communication.

In [2,3], the authors have proposed a constrained random stimuli and functional coverage formulation for a mixed signal verification, but, there is no clear methodology for a verification flow. Also, the articles were not targeted to complex circuits or systems.

Based on this the lack of a established methodology, the current paper proposes a structural mixed-signal verification flow joined with a Metric-Driven Verification Methodology, vastly used for digital verification [4-11]. We use a communication transponder as the study-case, although the methodology is applicable to any communication circuit containing both reception and transmission ends.

3. Interface Verification

A. Mixed Signal Verification Flow

In order to obtain a design without functional errors, a verification flow to a mixed signal was applied to a SoC called Potiguara, which is used in the Brazilian Data Collection System (SBCD) [12], and was developed during the IC Brazil Designer Training Program. The SBCD is responsible to process data received from Data Collection Platforms and send it to a Base Station Data Center, which is responsible to analyze them. The targeted module in this work is the Transponder IP block, part of the Potiguara, composed by digital, analog and radio frequency blocks.

The Transponder IP data flow can be illustrated in high-level view of the block diagram shown in Fig. 1 (a) and it helps to understand the traditional verification difficulties. The verification of the top circuit where analog and digital parts are integrated allows implicitly that the functionality of the digital-analog interfaces, highlighted by red circles, can be checked. In case the block verification process follows the flow in Fig. 1 (a), the analog ends (receiver and transceiver) must be stimulated by test patterns, what is a very complex process.

To perform the verification, an alternative signal flow was established as in Fig. 1 (b), connecting the transmitter with the receiver through a model, which contains environment effects (modeling the transmission channel). After established the signal flow, several digital stimuli are sent to Design under Verification, DUV, at its digital ends, in order to stimulate the design with the most varied test cases and coverage data are collected in the monitors.

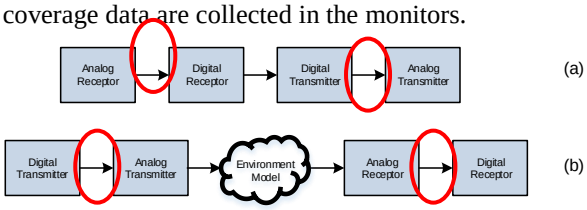

Fig. 1: *Transponder High Level Block Diagram*

B. Temporal Expression: Temporal Checks

In order to guarantee the protocol established among different blocks, a temporal expression called “expect” is defined with the objective to ensure that the interface will respect the protocol defined in the design specification.

The temporal checks are temporal expressions based on events that are emitted at the same time when the observed signal reach the expected value.

The verification environment developed using the e language [13] is composed by monitor, covers, BFM, checker, agents, eVC, drivers, sequence generator as one can see in Fig. 2. In the verification environment architecture, the temporal checkers structures are defined inside the monitors, which works as a passive unit with two main functions: the first one is to sample signals from DUV to send them to the checker and the second one is to evaluate the protocol of each DUV interface.

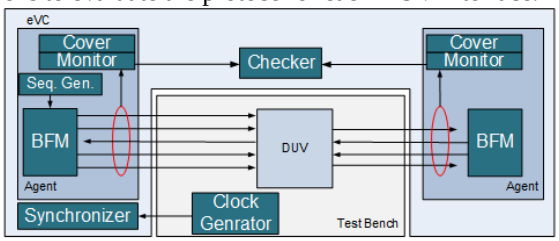

***Fig. 2**: Digital Verification Environment*

C. Coverage Plan

In the verification process, the functional and code coverage are metrics used to evaluate the efficiency of the test vectors applied to DUV.

In order to evaluate the verification process, the functional coverage of the Transponder top level are focusing on fields of the packet used to stimulate the DUV (sync word, sync bit, CRC and the size of the transmitted data).

4. Experimental Results

A. Analog Digital Interface Simulation

The interface between digital and analog blocks is a source of errors that need to be checked carefully during the verification process. Focusing on the interface, five temporal checks were defined in order to guarantee the correct operation of the interface. As an example, in the first part of Fig. 3 is shown the waveform in the interface between the Analog to Digital Converter (ADC) and the digital block called Window. In the second part of Fig. 3 it is possible to observe the protocol between two digital block, Window and a second block denominated FFT.

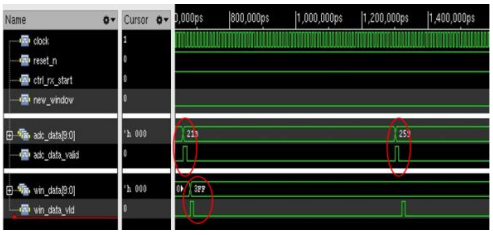

***Fig. 3:** Protocol Verification*

B. Coverage Extraction

The coverage was extracted using the tool Incisive Metric Center (IMC) developed by Cadence™ [13] - version 15.10-s007. With IMC the code and functional coverage analyses was performed while the test cases needed to be generated, in order to achieve a better coverage, was identified. In our experiments, a code coverage of 90,71% and a functional coverage of 95,6% was achieved.

5. Conclusions

In this paper, it was presented the challenges involving an interface between digital and analog domains as a target of a verification strategy in SoC composed by digital, analog and RF blocks, in particular, communication transponders.

The main key benefits in implementing this kind of verification includes: (i) simulation with integrated digital and analog components, (ii) interface analog digital protocol verification, (iii) real response by analog components, (iv) reusable digital verification environments, (v) fast simulation, (vi) functional and code coverage.

The future works will be focused in extending interface verification to SoC examples with a large number of interface between digital, analog and RF blocks.

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